PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G11B 7/14, 27/11, 27/36 — A1

(11) International Publication Number: WO 97/28530

(43) International Publication Date: 7 August 1997 (07.08.97)

(21) International Application Number: PCT/CA97/00069

(22) International Filing Date: 3 February 1997 (03.02.97)

(30) Priority Data:
9602213.2 — 3 February 1996 (03.02.96) — GB

(71) Applicant *(for all designated States except US)*: PARALIGHT LASER TECHNOLOGIES INC. [CA/CA]; 2nd floor, 1357 Bathurst Street, Toronto, Ontario M5R 3H8 (CA).

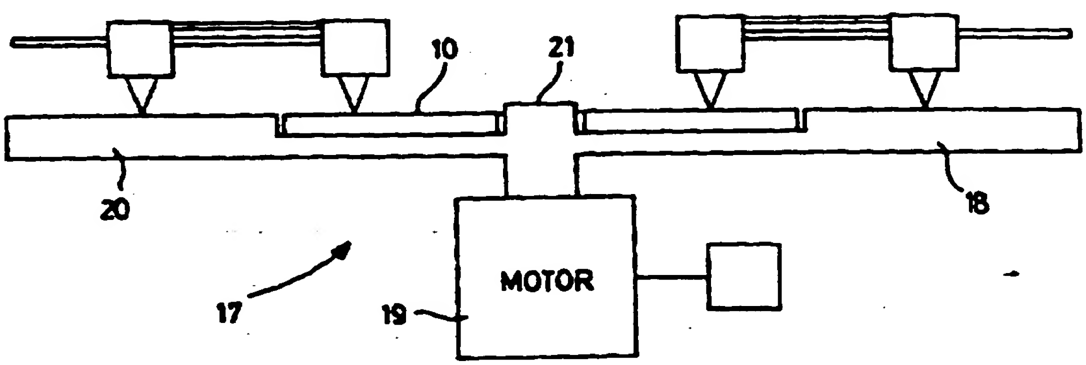
(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: DEWAR, Steven, W. [CA/CA]; 2nd floor, 1357 Bathurst Street, Toronto, Ontario M5R 3H8 (CA). REGAZZO, Ricardo [CA/CA]; 164 Dovercourt Road, Toronto, Ontario M6J 3C4 (CA). WILTSHIRE, John, H., D. [CA/CA]; 67 Marion Street, Toronto, Ontario M6R 1E6 (CA). SMITH, Gregory, L. [CA/CA]; 19 Humbercrest Boulevard, Toronto, Ontario M6S 4K6 (CA).

(74) Agent: ORANGE, John, R., S.; Orange and Associates, Toronto Dominion Bank Tower, Suite 3600, Toronto-Dominion Centre, P.O. Box 190, Toronto, Ontario M5K 1H6 (CA).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: MULTIHEAD RECORDING AND RETRIEVAL APPARATUS AND PROCEDURE FOR USE WITH SELF-TIMING OPTICAL LATHE OR PRE-FORMATTED DISCS



(57) Abstract

An optical drive to transfer data between a data carrier (10) and a data communication circuit is disclosed. The drive has a support to rotate said carrier about an axis and a plurality of optical head assemblies are disposed about the axis. Each of the head assemblies are radially adjustable relative to said axis to scan said carrier as it rotates. Each of said head assemblies has a clock recovery circuit associated therewith to obtain a clock signal for data processed by respective ones of the optical head assemblies. A plurality of data streams may be processed and their outputs combined to enhance the data recovery rate. The clock signals are derived from a timing track conjointly rotatable with the carrier and providing a clock signal correlated to the radial position of each of the heads. Each of the head assemblies includes a first head to read the timing track and a second head to interrogate the data carrier.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	GB	United Kingdom	MW	Malawi
AT	Austria	GE	Georgia	MX	Mexico
AU	Australia	GN	Guinea	NE	Niger
BB	Barbados	GR	Greece	NL	Netherlands
BE	Belgium	HU	Hungary	NO	Norway
BF	Burkina Faso	IE	Ireland	NZ	New Zealand
BG	Bulgaria	IT	Italy	PL	Poland
BJ	Benin	JP	Japan	PT	Portugal
BR	Brazil	KE	Kenya	RO	Romania
BY	Belarus	KG	Kyrgystan	RU	Russian Federation
CA	Canada	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic			SE	Sweden
CG	Congo	KR	Republic of Korea	SG	Singapore
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LR	Liberia	SZ	Swaziland
CS	Czechoslovakia	LT	Lithuania	TD	Chad
CZ	Czech Republic	LU	Luxembourg	TG	Togo
DE	Germany	LV	Latvia	TJ	Tajikistan
DK	Denmark	MC	Monaco	TT	Trinidad and Tobago
EE	Estonia	MD	Republic of Moldova	UA	Ukraine
ES	Spain	MG	Madagascar	UG	Uganda
FI	Finland	ML	Mali	US	United States of America
FR	France	MN	Mongolia	UZ	Uzbekistan
GA	Gabon	MR	Mauritania	VN	Viet Nam

MULTIHEAD RECORDING AND RETRIEVAL APPARATUS AND PROCEDURE FOR USE WITH SELF-TIMING OPTICAL LATHE OR PRE-FORMATTED DISCS

This application relates to optical recording and/or reading apparatus, collectively referred to as an optical drive.

PRIOR ART

Constant Linear Velocity (CLV) optical record carrier bodies, such as Compact Discs (CDs), employ a spiral track pattern which is typically read by scanning with a focused laser spot of approximately 800 to 1000 nm in diameter measured at the so-called "50% power radius". Conventionally, the spot is scanned along the path of a spiral track composed of data marks at a constant linear velocity, (e.g. either 1.4 or 1.20 m/sec in the CD system). Such CLV systems exploit this uniform scanning rate to increase data density by using a marking strategy known as Uniform Spatial Density (USD) by which data is recorded using marks of standardized lengths or channel bits which are typically organized in frames or data blocks of uniform length.

This strategy typically requires that CLV systems vary the spindle rotation rate in order to scan tracks formed at different radii. Thus, the spindle of a Compact Disc (CD) player, for example, rotates at approximately 8 revolutions per second (rps) while scanning the innermost part of a CD's data area and slows in a measured way, maintaining a constant linear velocity, to approximately 3.3 rps when scanning the outermost turns of the spiral track. In this case the constant linear velocity maintains a uniform frame rate and a constant channel bit rate of 4.3218 MegaHertz (MHz) throughout the entire 5.7 km length of the track. Such control of rotation and scanning rate is typically accomplished by recovering a clock frequency from the data recorded in the track and synchronizing the scanning rate with a clock crystal by means of a phase-locked loop.

It is well known that as a result of this arrangement, conventional CLV players and recorders can only operate one head at a time for recording or reading because only one point on the disc will have the rotation rate required to produce the requisite linear velocity..

To record optical data on a disc, it is possible to use one of several known approaches. Optical data track patterns are most often formed on truly featureless blank discs by so-called "mastering" machines which resort to various rotary encoders and linear

translation systems which are precisely coordinated by one or more microcomputers. As a general rule, such machines are too expensive for use as recorders of single copies of discs and are thus employed almost exclusively in the production of the master elements for injection molding. The so-called CD-R (or CD-RECORDABLE) systems operate as CLV read and/or write devices and so can operate on only one portion of the track at a given time. As a result, such devices are limited in the rate at which data can be recorded.

CD-R employs a pre-grooved track across the entire data area of the disc which is used to control its servosystems. The "track" of this recordable record carrier body takes the form of a spiral groove pattern which can be readily followed by the optical head of a CD-R recorder, guiding it to form an appropriate data spiral. This preformed spiral track is typically a groove formed to a depth of one-eighth the wavelength of the scanning laser spot (typically 1/8 of 780 nm). Also, this groove is formed typically so that it incorporates a radial wobble on the order of +/- 100 nm or less, which, when scanned at the specified linear velocity can be detected as a clocking pattern typically on the order of 22 kiloHertz (kHz). Detection of this wobble (for example, by a refined tracking error circuit) in effect serves as an indication of linear velocity and the wobble frequency can be synchronized with a much faster data clock during record operations. The groove may also be characterized to facilitate detection by a side beam formed by passing the spot through a diffraction grating but otherwise focused and positioned normally which is commonly employed in the method known as "3-beam tracking".

It is possible in some cases to employ only a timing wobble during recording and reading. While this has the virtue of minimizing inter-symbol interference which might interfere with readback data recorded on the drive such an approach has no address included in the track pattern. Such simple wobble patterns, or similar formats executed in other contrasting patterns. can be detected by the recorder and used to control the timely operation of the write laser in order to form pits of appropriate size in the area between the wobbled grooves. However, this approach to data timing is generally inferior to methods which establish track addresses in the data.

Most existing single head recorders designed for operation at a CLV have resorted to use of a track address pattern in the preformat structures in order to enhance reliability. In the case of CD-R for example, such preformatted address marks are typically referred to as ATIP marks which is an acronym for "Absolute Time In Pre-groove". High

speed single head recorders make increased use of ATIP marks in order to achieve sufficient accuracy and reliability of clocking functions. Indeed, this approach effectively uses the ATIP marks in the manner of the method known in the prior art as "Sampled Servo" control. In effect, an intermittent pattern (in this case, the ATIP marks) can be detected and used to maintain control of clocking and address functions. It can be readily understood how a combination of a recovered wobble track clock signal can be checked against a sampled servo clock signal in order to produce more reliable control of read and write functions.

Another fundamental approach to such control of track formation is disclosed in prior USP 5,303,215 for Self Timing Optical Lathe (or STOL) which also can be used to form CLV data pits in spiral tracks on either grooved or flat record carrier discs and which, since it dedicates far more data to the formatting encoder provides superior clocking and address resolution to the above approaches. One form of STOL utilizes a separate timing track or encoder disc having reference marks corresponding to a clock cycle at a correlated location on the data carrier. In this manner, the disc may be operated at constant angular velocity (CAV) but a timing signal may be derived for each position of a head.

There is a significant need for devices which can both record and read data from an optical disc at a high speed and considerable effort has been expended to that end. The basic approach which has been proposed to date is to speed up the operation of a single head optical drive. Such an approach may be employed with either CD-R or with the Self Timing Optical Lathe or STOL. STOL has the benefit of a clocking system which displays significantly greater resolution, robustness and reliability than that provided in the CD-R approach. However, for both approaches there appear to be physical limits to the speed with which spiral tracks can be read or written with a single head.

The speed of operation of a single optical head is limited by two key factors - namely, the opto-mechanical limit, i.e. the capacity of known tracking and focus actuators to execute the requisite repositioning and refocusing of the spot as track velocities increase, which limits both reading and recording apparatus, and the modulation limit, i.e. the speed at which laser diodes may be pulsed under sufficient control to form satisfactory marks, which limits recording operation. In the case of a Compact Disc for example, the disc is uniquely inserted each time it is read or written to. Inevitably, this means that the track

pattern on the disc will be more or less eccentric, and, typically, this eccentricity will produce the largest component of tracking error encountered by the head. It can be readily seen that, assuming an eccentricity of up to +/- 300 microns, an accelerated recording rate in combination with the variation in rotation rate required by CLV devices will dramatically increase the demand on the tracking actuator. This is especially true at the inner track radius.

If a track at normal CLV requires 8 rps rotation, then the rotation must be increased to 32 rps for a head operating at 4 times normal speed and to 64 rps for 8 times normal speed, etc. This means the actuator must be repositioned at a far higher speed which in turn requires switching currents that dramatically increase in magnitude with each increase in speed to be delivered through comparatively delicate actuator coils. This factor has been central to limiting the degree to which single head recorders can be speeded up.

For practical purposes, until recently the fastest CD ROM machine on the market operated at 6 times normal speed and the fastest prototype CD-R drives reported operated at 8 times the nominal operating speed. The first commercially available CD ROM drives operating near the theoretical upward limit have begun to appear. Even at these rates, the data transfer rate is below that considered desirable in many applications. There is therefore a need for an optical drive that may read and/or write data at an enhanced rate.

It is an object of the present invention to provide such a drive and obviate or mitigate the above disadvantages.

In general terms, therefore, the present invention provides an optical drive to record to and/or read from a data carrier optical data recorded as an optically detectable pattern of marks modulated in at a uniform spatial density. The data carrier is rotatable about an axis and a plurality of optical heads are circumferentially spaced about said carrier. Each optical head is radially adjustable relative to the carrier to scan said data carrier and has a clock recovery circuit associated with it to recover a clock signal from data processed by the optical head. Accordingly, a plurality of parallel data streams may be processed to enhance the cumulative data transfer rates.

Preferably, one of said clock signals is used to control rotation of said carrier and maintain said clock signal at a predetermined frequency.

As a further preference, said clock signal is derived from a timing track conjointly rotatable with said carrier and providing a clock signal correlated to the radial position of each of said heads.

Where a timing track is utilized, it is preferred that a pattern is utilized that provides a course clock signal with intermediate clock signals interposed between said course clock signals. The intermediate clock signals are preferably structured to accommodate the interrogating beam between the pattern.

It will be appreciated that there is substantial variation in linear track velocity for heads scanning at different radii in the data area due to the nature of the spiral track. Since the various spirals are all formed on the same disc and can only be rotated at one rate at any given time, a head positioned at a radius of 23 mm will encounter less track length during one rotation than a head positioned at radius 57 mm. Consequently, the uniform length of CLV track structures will be scanned by different heads at different radii at different rates. Specifically, regardless of the rotational rate, the outermost head will encounter the fastest linear velocity and hence the fastest channel bit rate while the innermost head will encounter the slowest linear velocity and channel bit rate. Further, assuming any number of heads are employed in a multiple head drive, only one can operate at a constant linear velocity and all of the others will encounter variable linear velocities.

Conventional systems decode or write data tracks by comparing linear scanning velocity to a system clock. In the CD system for example, a 4.3218 MHz clock signal is used to discriminate between the shortest pit pattern (a so-called "I-3") and the next longest pit pattern (a so-called "I-4") by detecting that the transition from pit to land (or, vice versa) occurs during one clock cycle as opposed to another. That is, one clock cycle corresponds to one third of the shortest channel mark or on the order of 290 nm. Accurate recording typically requires pit edge formation on the order of +/- 50 nm. In a system such as the CD platform with a track pitch of 1600 nm, each track spiral will vary in length from the adjacent spirals by approximately 10,000 nm or fewer than 35 Channel Bit/Clock cycles.

It will readily be seen that this uniform track-to-track variation impacts tracks which vary far more substantially in length at different radii very differently. While it is theoretically possible to calculate the relative clock frequencies required for the operation of multiple heads from a system clock with sufficient accuracy it does not appear to be

practical, especially given tolerances for tangential marking of pit edges is only +/- 50 nm and smaller in proposed systems.

By providing each head assembly with a clock recovery circuit, individual data streams may be recorded and/or recovered and subsequently utilized.

Where a separate timing track is utilized, the clock recovery may be enhanced by utilizing a specific timing pattern that matches the characteristics of the interrogating beam.

Embodiments of the invention will now be described by way of example only with reference to the accompanying drawings, in which

Figure 1 is a plan view of an optical disc drive and data carrier;

Figure 2 is a side elevation of the drive shown in Figure 1;

Figure 3 is a plan view showing the configuration of a data carrier and data encoding pattern;

Figure 4 is a plan view similar to Figure 1 showing the relationship of the optical disc to a single recording/reading head;

Figure 5 is schematic representation of a data structure used on the disc and data encoding pattern;

Figure 6 is a schematic circuit diagram showing the extraction of the clock cycle from the data encoding pattern.

Figure 7 is a schematic diagram of a control for the motor shown in Figure 1;

Figure 8 is a further embodiment of the control for the motor shown in Figure 1;

Figure 9 is an alternative embodiment of the control for the motor shown in Figure 1;

Figure 10 is a schematic illustration of a data recording arrangement;

Figure 11 is a schematic side elevation of an alternative arrangement of encoding disc; and

Figure 12 is a side view showing a further form of encoding disc.

Referring therefore to Figures 1-4, an optical data carrier 10 has a data carrying area 12 located between radially inner and outer extremities 16. Carrier 10 includes a central hole 11 and an outer periphery 13 to conform to standard physical

dimensions for an optical data carrier and data is stored on a spiral track 14 as a series of pits and lands that represent sets of data channel bits and which are combined as frames of predefined format as is well known.

An encoding disc 20 is located radially outwardly of and concentrically with the carrier 10 and is formed as a permanent part of an optical drive 17 that may both record and read data on the track 14. The drive 17 includes a motor 19, support platen 18 and spindle 21 as will be described more fully below. Disc 20 is incorporated into the platen 18 so that data carrier 12 and disc 20 are generally concentric to the spindle 19. The encoding disc 20 has an encoding area 22 located between inner and outer extremities 25 that has the same radial extent as the data carrying area 12.

The encoding area 22 is formed with an optically addressable spiral track 29 having a pitch corresponding to the pitch of the track 14 and carries timing marks having a direct relationship to the length of track 14 occupied by sets of channel bits. For a CLV track, the length of track 14 occupied by one frame or data block remains constant along the track. Because the track 29 is offset radially relative to the data carrier 10 the length of each mark on the track 29 will be factored relative that on the data carrier by the ratio of the radiuses. In this manner, the angular rotation of the data carrier 10 necessary to scan one channel bit of track 14 will correspond to the angular rotation necessary to read a timing mark corresponding to one channel bit on track 29. At any given radius, the timing mark may b scanned to derive a waveform of sufficient precision to derive a timing signal related to the fundamental channel bit length of the data signal.

The signal derived from track 29 is called a "pseudoclock" and, as it is a physical measurement of rotation that is encoded in a manner which corresponds to each track rotation to be recorded on the target disc, it serves as an alternative means of measuring channel bit length which is independent of the track scanning velocity.

For example, a data carrier 10 bounded by an outer radius R_o and an inner radius R_i in Figure 3 is recorded with a spiral track 14 in the data area 12 lying between radius 22.5 mm and radius 57.5 mm. A pseudoclock pattern in the form of spiral track 29 on the encoding area 22 is offset radially 47 mm from the position to define an annulus between the extremities 25 having approximate radii of 64 mm and 114 mm respectively. The track 29 has the same spiral pitch (1.6 μm) as that of track 14 of the data carrier to be recorded and is marked off in circumferential sections which correspond to the rotation

necessary to scan each relatively offset CD data frame. In this manner, every CD frame on track 14 has its own correlated radially offset frame on the track 29. Each offset frame may be further divided into a plurality of offset marks which can be used to measure an appropriate circumferential location for any combination of the potential pit/land transition points which may be encoded on data on the track 14.

Thus, as shown in Figure 3, arc 7 on the spiral track 29 can be seen to be a radial offset of arc 8 representing a frame on track 14 and it can be understood that each channel bit in the entire data pattern to be recorded in the CD data area 12 has a corresponding location on the track 29.

The form of data pattern employed on the track 14 and track 29 is shown in Figure 5. The data format employed on track 14 is shown in Figure 5a where each frame as represented by arc 8 includes a pair of synchronizing blocks 27 each formed from 11 channel bits having track length Tc. The synchronizing blocks 27 are followed by a subcode block 28 formed from 14 channel bits and 3 merging bits and a data block 30 configured as a series of data words formed from channel bits. Each frame therefore includes 588 channel bits.

The corresponding frame on the track 29 is shown as Figure 5b where the segment Tcc represents the length of track 29 corresponding to the channel bit Tc at the offset radius. The track 29 is formed with synchronizing blocks 62 followed by a subcode block 68 and a data block 30a which is formed with a uniformly repeating pattern to provide a repetitive clock-like signal. Rotation of the support platen 18 to scan one channel bit Tc will cause a corresponding rotation of the encoder disc 20 to scan the radially offset channel bit Tcc. When the track 29 and disc 10 are co-rotated, scanning of the pattern on track 29 can yield a measure of all required pit/edge locations on the track 14 regardless of scanning rate.

As can be seen in Figure 1, a plurality of head assemblies 33 are circumferentially spaced about data carrier 10. Each head assembly 33, which is shown in greater detail in Figures 2 and 4, is radially movable in a support 32 and its position is monitored by a position sensor 31. Each head assembly 33 includes a pair of optical heads 34,36 which are spaced apart a fixed distance corresponding to the radial spacing of the inner extremity 16 of the data carrying area 12 and the inner extremity 25 of the track 29 area. The two heads 34,36 are mounted on a common radial support 32 and their position

can be manipulated by a coarse positioning actuator 35. Both optical heads 34,36 are equipped with a fine positioning/focusing actuator typically referred to as a two-dimensional actuator (or 2-d actuator) such as is well known in the art. The head 36 is a READ/WRITE head which addresses the data carrier 10 and the head 34 is a tracking and timing head which addresses the track 29. The READ/WRITE head 36 may be capable of Read-After-Write operation or of simply reading data already recorded on the target disc by reference to the pseudoclock.

Initial adjustment of the offset between heads 34,36 of the head assembly 33 is obtained by moving the two heads 34,36 to address two offset alignment tracks 50,51 formed on inner and outer peripheries of the encoder disc 20. The tracks 50,51 are radially spaced by the offset between a track on the disc 10 and the corresponding track on encoder 20. This provides an initial alignment for the heads 34,36 prior to reading respective patterns. The alignment tracks 50,51 are recorded as track patterns radially offset from the other and recorded on the encoder disc 20 as part of the recorder 17.

As the encoding disc 20 and the data carrier 10 are co-rotated on the spindle 19, the two optical heads 34,36 scan the tracks 29,14 respectively. For each radial position of the head 36 on the data carrying area 12, the head 34 is located at a correlated location on the encoding area 22 and the timing mark recorded at that location on track 29 is used to demodulate the data. Assuming that the carrier 12 has data recorded, as the data carrier 10 is rotated, each head 36 will read the corresponding portion of the data track 14. A timing signal will be obtained from the head 34 scanning the encoder track 29 and the data stream demodulated as described with reference to the circuit shown in Figure 6.

As the pseudoclock reference is a measure of spatial positioning along the spiral rather than a time-based clock signal, it permits a number of heads to be operated at the same time at different radii with different and varying linear scanning velocities and provides an appropriate demodulating clock signal for each location.

Referring to Figures 5 and 6, the pit pattern formed by a single offset data frame on the track 29 as shown in Figure 5b is an idealized representation of the electrical signal produced by the photodiodes associated with the optical head 34 while scanning the pit pattern on track 29 on the encoding disc 20 with a focused laser spot. The signal read from track 29 on the encoder disc 20 is fed to a clock pit extraction circuit 48 which can identify the synchronization blocks 62 directly or by means of run length violations. Such a

clock pit extraction produces a signal such as that shown in Figure 5c. The extracted clock pit signals are then fed to a clock synchronization circuit such as that shown schematically in Figure 6.

The output of extraction circuit 48 is fed to a phase detector 50 before passing through a low pass filter 54 to a voltage controlled oscillator 55. The VCO 55 is coupled to a divide-by-n counter 56 which is in turn linked to the phase detector 50. In this manner, the frequency of the VCO 55 can be controlled so as to produce a pseudoclock output which is equal to, or a multiple of the local channel bit rate associated with any given frame. The output of VCO 55 is applied to the demodulation circuit 57 that also receives data from the track 14.

Accordingly, at each location, a clocking signal is provided that is representative of the channel bit length at that location and the linear velocity at which the record is being scanned by that specific head. The clocking signal is applied to the data stream recovered from the track 14 by the associated head 36 to recover the channel bit stream. Each head is therefore able to recover from or record to data recorded on the track 14 of carrier 10 and provide multiple data strings that can be combined serially or processed in parallel.

The VCO circuit may also incorporate a secondary phase comparison circuit indicated at 58 which can detect the pattern produced by scanning the pseudoclock pattern between the synchronization marks and such a circuit may further refine the frequency control of the VCO 55 so as to keep it more closely aligned with the linear track velocity and hence improve pit location and measurement on the target disc. Such systems may be further refined by resort to circuits employing various digital filtering techniques including application specific digital signal processors in procedures which are generically referred to as PRML, (partial-response maximum-likelihood), channels. and, by variations on such approaches which are referred to as Adaptive PRML.

Such techniques are particularly useful for resolving Inter Symbol Interference, (ISI) by incorporation of a sample detection scheme which typically filters analog read-out data once per clock cycle as opposed to traditional continuous-time zero-crossing detection. Such a system typically detects so-called "Channel Samples" and employs them in a digital filtering scheme whereby each analog sample from the read-out signal is compared once per bit time with each adjacent sample.

A number of existing schemes for discriminating analog data patterns from ISI and other forms of interference have been demonstrated and may be employed here. Such systems have been employed in both conventional magnetic hard drives and in magneto optical drives in configurations which call for enhanced data recovery due to ISI and essentially enhance retrieval of data. In the case of the current invention, such means may be employed to enhance recovery of the linear track reference whether it is encoded on the target disc or on a displaced encoder disc.

Similarly, non-linear pseudoperiodic circuits such as those disclosed in various papers, notably by T.L. Carroll and L.M. Pecora of the Naval research Lab in Washington D.C. disclose techniques by which to cascade synchronized chaotic systems in what they have termed the "chaotic analog to a phase locked loop", may be adapted for use in synchronizing the linear track position by locking the recovered frequency pattern detected by the scanning optical head from the encoder disc 20 to a VCO frequency.

With respect to recovery of the clock reference encoded in a CD-R disc it appears that a system which employs a PMRL scheme or cascaded chaotic system based clock recovery may be preferable.

It is possible to fabricate an offset timing track 29 with the conventional CLV characteristics to support multiple head operation. However, it is preferred that the pit pattern is enhanced in order to improve the clock recovery for multi-head operation.

Analysis of the requirements of the multi-head machines indicates that while conventional CD pit patterns are sufficient to derive the timing signal during CLV operation they do not provide optimal pseudoclock data for timing multi-head operations. During conventional CLV scanning, the frame synchronization marks can be phase-locked to a crystal clock and the product of a divide by 588 counter can thus be stabilized to produce a working clock signal. However, in multi-head operation a crystal clock cannot be employed.

The problem is tied to geometry. If the outermost head is scanning or writing between radius 49 mm and radius 58 mm the change in linear scanning velocity for the innermost head scanning between radius 22.5 mm and radius 31.5 mm during the same operation will change dramatically. As a direct consequence, the clock rate of the data varies dramatically as well because in a CLV system the clock rate is a constant relative to track velocity. In the case described above, the linear velocity and the spatially demarcated

clock signal change on the order of 20% during the period that the 9 mm of tracks are scanned. Similarly, if the clocking signal is tracked by a Voltage Controlled Oscillator (VCO), the VCO must be able to recover a pseudoclock signal over a range of about +/- 9% around its center frequency. Any such VCO loop must be made unacceptably "loose" if it is to follow the variations in scanning rate using a reference pattern as diverse as a normal EFM pit pattern. It would appear that there is simply not enough clocking or, more precisely, enough detailed linear positional data in a conventional EFM pattern with which to operate conventional circuits.

Experimentation with various loop designs indicates that, in effect, conventional EFM loop reference provides insufficient resolution for use with conventional zero-cross detection of such timing data because the derived pseudoclock frequency drifts for lack of correction in the operation. It is possible to incrementally vary the loop constants of the VCO with sufficient accuracy to control READ-only operations in, for example, the demodulation of the EFM data (eight to 14 modulation) used in the compact disc system because the system makes heavy use of error correction. As a consequence, substantial errors in the recovery of the data clock may be overcome by the operations of the CD-DSP in a manner similar to the way in which the system deals with scratches and other flaws in the data track. However, this is not the case for WRITE operations because, obviously, the system cannot make reference to error correcting patterns recorded in pits which it is writing. As a consequence, such adjustments are hampered by variations in spindle speed caused by CLV operation (phase jitter) and the lack of an adequate clocking or linear track encoder pattern that the derived frequency is still not adequate. In fact, the requirement for keeping the preformat marks from interfering the normal read out of data to be recorded makes it difficult to recover an adequate clock reference for single head CD-R drives operating at CLV. Such problems are not alleviated entirely by operating the turntable at a constant rotational rate.

These limitations apply in a less stringent form as well to the use of an offset encoder disc for the derivation of the variable frequency of pseudoclock.

This limitation is a direct function of the limited degree to which the clock content expressed in an EFM pattern can be used as a linear track encoder. Moreover, EFM code like any optical data recording pattern employs a data slicing technique which requires a long integrator in the circuit in order to determine the so-called "zero-crossing" point or

"slicing level" which marks a transition from a pit to land. As a consequence, such pit/edge transitions can only be detected with limited, and insufficient accuracy. This operational parameter is a function of the DC balancing of the pit/land pattern which uses a comparatively crude measure known as the "Zero Sum Factor".

To enhance the clock recovery, it is preferred that the track 29 has the following characteristics. The accuracy with which the pits can be scanned is a function of the size of the pits relative to the size of the laser spot, or, more precisely, the size of the 50% power radius of a focused spot. In the CD system, the smallest pit or land is approximately 890 nm in length and the 50% radius of the focused spot (which has a wavelength of 780 nm) is on the order of 1000 nm. This produces the minimum contrast, (or, "I-min" as it is usually referred to), specified for a system using analog scanning techniques, (eg. continuous-time zero-crossing). Similarly, there is point beyond which increments in pit length do not appreciably increase the contrast between pit and land. This maximum contrast, (or "I-top" as it is known, occurs with pits or lands which are on the order of 1800 nm or larger because the light within the 50% power radius of the focused spot no longer spills over from one feature to another but, rather, is fully on or off such a feature. As the spot is scanned, the transition point can be more reliably detected despite normal operational limitations caused by momentary defocusing of the spot, comat error, etc.

Hence, to improve clock recovery from an encoder disc 20, the pit pattern on track 29 is predominantly composed of pits of 1800 nm or more in length. This dramatically enhances the capacity of the optoelectronic circuits to detect transitions. It also means that the track, for the most part, avoids the use of Offset I-3 marks because for the most practical offset pattern formations such marks are shorter than 1800 nm. More generally, the pits have a length when measured in the direction of the track 29 greater than the 50% power radius of the focused spot.

Specifically, as shown in Figure 5b, the preferred pit pattern employs radially offset pits each of which corresponds to 4 clock cycles, i.e. 4 Tcc, to make up more than 90% of each frame. Such pits satisfy the contrast detection criteria specified above.

As shown in Figure 5b, each radially offset frame indicated at 60 is a radial offset of a 588 Channel Bit CD frame. The head of each frame is composed of a radially offset pattern of one synchronization block 62 (composed of one 11-clock cycle pit 64 and

one 11-clock cycle land 66) followed by a sub-coding block 68 made up of a combination of pits and lands such that the block 68 will not be longer than 14 clock cycles. The subcoding block 68 typically contains serial data which encodes address information. The balance of the frame 60 is composed of 138 pit/land patterns 70, each a radial offset of 4 channel bits. In sum, each frame will contain 588 offset channel bits (OCB) in the following pattern:

SYNCHRONIZATION BLOCK:	(2 x 11 OCB)	= 22 OCB
SUBCODE BLOCK:		= 14 OCB
PSEUDOCLOCK PATTERN:	(138 x 4 OCB)	= 552 OCB
TOTAL		**588 OCB**

The recovery of the clock signal is further enhanced by using a specialized subcode pattern in the subcode block 14. The DC content of the photodetectors used in optical scanning never goes through zero because some light is always reflected from the lands between adjacent passes of the track and the portions of the spot which, though below the 50% power level, nevertheless spill over into the lands between pits. This is ameliorated in the in-track direction, (what is referred to as "inter symbol interference" or ISI), by the comparatively large scale of the features of track 29 but only to a limited degree transverse to the track because the track pitch of 1.6 μm is identical to that employed on standard CLV devices which produces comparable cross talk and reflection from the lands between tracks. An active "data slicer" is used to determine the zero crossing level between a pit and a land in a manner comparable to that employed in a conventional player.

To avoid "jitter" of the zero crossing the pit pattern in track 29, a "self-balancing code" is employed to provide a D.C. Zero sum. Specifically, each track structure will be self balanced, that is, there are an equal number of offset channel bits forming the pits and lands in each pattern as follows:

SYNCHRONIZATION BLOCK

11 OCB PIT	= -11
11 OCB LAND	= +11
D.C. BALANCE	= 0

PSEUDOCLOCK BLOCK 30a (ALTERNATING 4 OCB)

69 X 4 OCB PITS	= - 276
69 X 4 OCB LANDS	= +276
D.C. BALANCE	= 0

SUBCODING BLOCK

14 bits representing one of 12 x 8-bit
word arrange in self-balance patterns

The subcode block contains address information and requires a total of 12 pit/land patterns to produce 2 Subcoding sequence patterns (S1 and S0) which denote the start of blocks of sequential data, and 10 self-balancing data words each of which represents a number. The following is only one possible version of such a self-balancing code. The important features are that whatever pattern is employed should be self-balancing with respect to pit/land lengths, and, should be reasonably efficient so as not to unduly reduce the total length of data block 30a available as offset pseudoclock reference within each channel bit frame.

In the preferred embodiment laid out below, the self-balancing code is expressed as two characters: the first a numeral; the second either a "P" or an "L". The numeral indicates the number of clock cycles required to scan the feature at normal CLV and the P and L represent whether the feature is either a Pit or a Land respectively. Thus S1, for example, is described as "7P/7L" meaning it is the radial offset of a pattern of a pit 7 standard CLV Channel Bits in length and a land 7 standard CLV Channel Bits in length which, when scanned would have a "Zero Sum" as such a conditional DC balance is usually described:

PIT PATTERN

S1 (SUBCODE START)	7P/7L
S0 (SUBCODE START)	2P/2L/5P/5L
1	2P/5L/5P/2L
2	5P/5L/2P/2L
3	3P/3L/4P/4L
4	3P/4L/4P/3L
5	4P/4L/3P/3L
6	5P/2L/2P/5L
7	4P/3L/3P/4L
8	3P/3L/2P/2L/2P/2L
9	2P/2L/3P/3L/2P/2L
0	2P/2L/2P/2L/3P/3L

Employed with a serial data encoder/decoder circuit, such patterns can be used to readily derive six 8-bit words which can be recovered sequentially from the 14 channel bits forming each subcode block 68 as a number taking the form XX, xx, *xx*. Where:

XX = Absolute Minutes
xx = Absolute Seconds
xx = Absolute CD Frames

The conventional compact disc system groups the 588 bit frames into blocks formed from 98 frames or 57,624 channel bits. This not only provides 98 subcode blocks 68 in each block but the recovered address used in conjunction with a frame counter and, if desired a channel bit counter, can be used to resolve the address of every channel bit edge over the entire 5.5 km of track to a resolution of +/- 50 nm.

As the preferred embodiment only requires six patterns in the subcode to identify an address, there is ample room within the serial data structure of 98 frames to build redundancy which will protect against error. The preferred embodiment includes provision for such redundancy in the following manner:

1. The first subcoding mark, S1, followed in the next frame (i.e., 588 channel bits later) by the second subcoding mark, S0, indicates the start of a subcoding sequence.

2. Minimal provisions for cyclic redundancy will be made as only positional data is encoded and each block (i.e., each 98 frames) forms a portion of a linear sequence with that preceding it and that which follows.

3. At the mid-point (i.e., at the 49 frame) of each block, the subcode sequence will reverse such that SO precedes S1 to signal the beginning of a redundant series.

By utilizing the above format for the track 29, an accurate clocking signal is obtained and an address indicative of the position along the track, and hence the radial position is obtained.

The use of a separate timing track also increases the versatility of the record/playback device by accomodating both scanning rates found on CDs.

The Compact Disc system utilizes one of two linear scanning rates, the first being 1.4 meters per second and the second being 1.25 meters per second, (m/sec). Both systems are designed to be demodulated by conventional devices using a phase-locked loop and crystal clock running at 4.3218 MHz or some multiple thereof conventionally referred to as 2x, 4x, etc. The difference between the standards is strictly linear: The 1.25 m/sec tracks employ 588 Channel Bits per Channel Bit frame but use proportionately smaller patterns. This means that 1.4 m/sec marks are proportionally longer as 1.25 m/sec marks.

As a consequence of this linear relationship, it is possible to use a pattern formed on track 29 to a 1.4 m/sec standard as a linear encoder in order to stabilize the generation of a frequency suitable for a m/sec recording operation. As shown in Figure 6, a frequency converter 70 is included to convert the scanned pseudoclock signal/derived VCO frequency such that 112 clock cycles are generated for each 100 recovered cycles of pseudoclock data formed at an offset at 1.4 m/sec. The data recovered from track 14 may therefore be demodulated at the required frequency. The frequency conversion may be accomplished in one of a number of known manners and is, of course, switchable upon the standard being detected.

The unused portions of the 98 frame subcode sequence may then be used to encode a 1.25 m/sec address sequence of exactly the same sort as the XX = Absolute Minutes, xx = Absolute Seconds, *xx* = Absolute Frames discussed above by incorporating two additional Subcoding mark sequences such S1/S1 or S0/S0 as sequence start marks for what may be considered a 1.25 m/sec subcoding channel. As the relative positions of each pattern bear a strictly linear relation to the other, a 1.25 m/sec subcoding channel can employ such a sequence start mark at the same point in the 1.4 m/sec sequence once every 28 frames, after which sequence initiation the serial data may be encoded in that sequential position relative to subsequent 1.4 m/sec sequential data. A circuit which compares the relative frame counts can provide a further redundancy check and/or 1.25 m/sec positional address as desired.

Importantly, the self-balancing code discussed above with respect to Figure 7 also makes it possible to refine the control of the data slicer circuitry and hence to more accurately measure pit/edge locations. This in turn facilitates the recovery of a more precise pseudoclock signal by means of a primary phase-locked loop which acquires coarse synchronization of a VCO frequency with that of the recovered pseudoclock signal from the disc. This is implemented as a circuit which recognizes the I-11 synchronization blocks 62 and pulls the VCO frequency into approximate phase using a divide-by-588 counter. Once this has been accomplished an edge triggered phase-detector corrects for phase by comparison of the VCO frequency and that derived from the I-4 clock pattern which comprises the bulk of each frame. In effect, the edge comparison continuously adjusts the frequency produced by divide-by-588 counter, keeping it fine tuned relative to the pseudoclock recovery signal. The divide-by-588 signal produced by the divider is maintained continuously so it functions, in effect, as a "flywheel" during the periods when synchronizing and address bits are being recovered.

The pseudoclock recovery circuit may also incorporate a programmable resistor which can be employed to adjust the phase-locked loop parameters in such a way that the VCO center frequency can be adjusted electronically to maintain “tighter” loop operations.

The subcode addresses are recovered using the circuit of Figure 6. As the pseudoclock VCO frequency becomes finely locked, it is applied to the subcode demodulation component 84 of the circuit. A subcoding sequence is detected by pattern

recognition circuit 86 enable by the frame pulse 82. When subcoding blocks S1 and S0 appear in the 14 Channel Bit space reserved for subcoding data in two successive frames, the circuit begins to assemble in register 88 the serial data which comprise the address. Each successive subcoding block is measured by comparison to the pseudoclock VCO frequency.

Recognition of a specific subcoding pattern by pattern recognition 88 results in the storage of an 8-bit digital word in register 88. After six 8-bit words have been derived from six successive frames, the register signals the system controller, preferentially a microprocessor, that a frame address has been received. The controller is then enabled to poll the register 88 in order to retrieve the address. The circuit is driven asynchronously by the recovered pseudoclock signal from VCO during its READ operations and is configured so as to deliver address data out to a system microprocessor as required. Provision may be made so that data being retrieved will be reclocked to conform with a standard crystal clock frequency suitable for communication with the system controller.

Each of the heads 34 recovers an address from the subcode in the portion of the track 14 being read by that head so that the system controller can identify the relative positions of the head assemblies at any given time.

It will be seen therefore that each head obtains an accurate clock signal from the track 29 that may be used to demodulate data recovered from the track 14 during reading or modulate data to be recorded on the track during WRITE operations. By utilizing the balanced code, a clock signal with enhanced accuracy is obtained and the address is readily retrieved for each block.

As noted above, two factors limit the performance of the drive, namely the limits imposed by the opto-mechanical system, such as the track and focus subsystems, or the limits imposed by the electro-optical system, such as the ability to read and write data. The limits imposed by the opto-mechanical systems are essentially independent of the rate at which data is read and depend more upon the angular velocity. The demands placed upon the opto-mechanical system tend to be greatest at the radially innermost track and accordingly where the opto-mechanical system is the limiting factor, control should be accorded to the radially innermost track.

Conversely, where the electro-optical systems impose the limits, the data rate is greatest at the radially outermost track being read and therefore it is appropriate to provide control to the radially outer head.

Control of the motor may be affected in a number of ways, as described below with reference to Figures 7-10.

Referring therefore to Figure 7, the clock signal recovered from each of the heads 33 are fed to restrictive comparators 90. Each of the comparators also receives the reference clock which corresponds to the designed CLV rate. The comparators 90 provide respective error signals indicating whether the recovered clock signal is less than or greater than the reference clock. The output signals 92 are supplied to an arbitrator 94 which determines which of the signals will be used for control purposes.

The arbitrator provides a control signal 96 to the control of the motor to adjust the rotational speed.

The arbitration performed by the arbitrator 94 will depend upon the limiting factors of the system. Assuming that the electro-optic factors, i.e. the data rate, is the limiting factor, the arbitrator will provide a signal at the output 96 causing the motor to increase speed so long as each of the recovered track clocks is less than the reference clock. As the outermost head attains a data rate corresponding to the CLV data rate, its control signal 92 changes from a speed-up to a slow-down signal. The arbitrator detects the change of state, which may be simply a voltage threshold level, and utilizes the control signal 92 as the output to control 96.

If the controlling head switches to a new radius so it is no longer the radially outer head, the error signal will again call for an increase in motor speed and the arbitrator will adjust the motor speed until a slow-down signal is received from one of the other heads.

Similarly, if the drive is limited by opto-mechanical factors, the arbitrator will cause the motor to increase speed until each of the comparators 90 provides a slow-down signal. In this case, the arbitrator accords control to the last head to issue the slow-down instruction.

In the embodiment shown in Figure 8, the address recovered from the track 29 is utilized as a control function. The address read by each of the heads 33 is supplied from an address register 100 to a comparator 102. The comparator 102 compares each of the addresses and determines which address represents the greater radial position. The head having the greatest address is selected through a channel selector 104 so that the data clock associate with that head is fed to a comparator 106. The comparator compares the data

clock with the reference clock indicating the designed CLV rate and issues an error signal at 108 to the control to adjust the motor speed accordingly.

Naturally, if the control is provided by way of the innermost track, then the comparator 102 will select the lowest address for control.

Further use may be made of the recovered address from the timing track using the control illustrated in Figure 9. In the embodiment of Figure 9, each of the addresses is recovered from a register 110 and provided to a look-up table 112. The look-up table 112 stores a spin rate for the motor to achieve CLV for each address. Each of the addresses from the address registers 110 retrieves the requisite spin rate and a comparator 114 determines which of those spin rates is appropriate. In the case of the electro-optical limits, the spin rate selected will be a minimum spin rate; where the opto-mechanical factors limit the operation, the spin rate selected will be the maximum. The comparator 114 outputs the selected spin rate to the motor for control.

The position of the multiple heads 33 provides a number of different operating parameters. Each of the heads 33 may be used to supply a data stream retrieved from the carrier 12 to independent sources. In this case, each communication channel operates independently at the data rate recovered from the carrier. If the data rate is to be provided at a fixed predetermined rate, then the communication channel may include buffering that permits the temporary storage of data that could be clocked out at the required rate. Where the heads supply a common communication bus, the data stream may be buffered and directed onto the communication bus under the control of the buffer either at a constant clock rate or as an asynchronous transfer at the clock speed recovered from the track 29. By monitoring the contents of the buffer, access to the communication bus can be controlled and maximum data transfer rate attained.

In some circumstances, as will be described further below, control of the contents of the buffer can be achieved by causing a head to rescan or delaying scanning of the tracks so that the buffer is not caused to overflow.

The above description has assumed that data is being read from the carrier but as noted above, the drive may be utilized to write data to the carrier 12. A particular benefit of such a device is for a point-of-sale manufacturing where selected data is to be written to an optical carrier to a customer's selection.

Despite the reduced requirement of spindle control accuracy using a STOL lathe, it is still necessary to provide a spindle motor control circuit capable of controlling spindle motor rotation rate in response to the recovered pseudoclock signal on the encoder disc 20. A number of different strategies are available depending upon system considerations as described below with reference to Figures 7-9.

Control and co-ordination of the various subsystems require the development of a dedicated microprocessor for the multiple head system as a whole. The preferred embodiment incorporates separate microprocessors for each stage which are soft programmed at start-up by the microprocessor and which control positioning, data timing and fine control of the write pulse. It will be understood that such operational controls can be configured in a number of ways known to prior art.

In fact, the development of many different configurations commercial multi-head, READ-ONLY, WRITE-ONLY, and READ-WRITE machines in various independent and/or parallel operating configurations will require the application of different software in some cases and in others different microprocessor systems controlling different elements of servo-systems and data handling.

4 HEAD PARALLEL WRITE machines configured for point-of-sale manufacturing will operate at cumulative rates from 12-60 times that of a normal CD-R recorder by utilizing four to twelve heads, each of which will write a portion of the track data area 12 between radius 22 mm and radius 58 mm in the following manner. Only the four-head (12 times normal rates) machine is considered here.

Each of the WRITE heads to be deployed for parallel operation must address a portion of the data area 12. As the track pitch is a uniform 1.6 microns per rotation, and all of the heads are addressing the same rotating surface, each goes through the same radial translation. Therefore, the approximate area recorded by 4 heads operated in parallel is as follows:

HEAD # 1: Radius 22 mm to radius 31 mm
HEAD # 2: Radius 31 mm to radius 40 mm
HEAD # 3: Radius 40 mm to radius 49 mm
HEAD # 4: Radius 49 mm to radius 58 mm

The use of multiple heads to write simultaneously to respective bands on the data carrier requires matching of the recorded data for continuity. In a four head CD recorder system in which each head is assigned to WRITE a track section with a radial area of approximately 9 mm, it will be noted that HEAD # 1, (the outermost head) is directed to a radius of approximately 49 mm. This position can be acquired in the preferred embodiment by executing a series of single track kick pulses in co-ordination with the encoder disc 20 in order to compensate for contrary radial translation during repositioning. The location from which to begin the kick pulse repositioning can be readily determined by reference to end marks in the preformatted track or by the end position of track 29. HEAD # 2, the next outermost head is also addressed to this address and reads the data which HEAD #1 begins to WRITE. In effect, this written pattern and the address on encoder disc 20 can now be closely correlated. As HEAD #2 reads the start of HEAD #1's track, it can correlate the position it finds the track with the position it would have placed it if it had been the first to write. In this way, radial and offset misalignments may be compensated for electronically.

HEAD #2 is then directed by kick tracks to its start position at a radial position about 9 mm closer to the center (at about r= 40 mm). By recourse to the read-out from lens position sensors in each head, it is possible to determine whether the radial offset between the encoder head and the write head are maintained at a constant offset in order to provide a check on the accuracy of the kick track positioning count.

The process used to reference HEAD 1 and HEAD 2 is now repeated to reference HEAD 2 and HEAD 3 at the 40 mm radius, and then repeated again referencing HEAD 3 and HEAD 4 at the 31 mm radius, and finally to position HEAD 4 at its start position at 22 mm.

In this manner, the encoder and address structure can be employed to address two or more heads to write any portion of a preformatted spiral track represented by any radial section of the preformatted spiral track.

A similar technique may be used on a single head to obtain continuous data recordal if even when the recording process is interrupted, such as for an archival process.

The ability to reposition a head assembly from the address of a previous track may also be used to interrupt scanning, such as when a buffer is full, and recommence

scanning when the buffer permits.

The degree of precision with which the track matching is accomplished may be varied according to the requirements of the recording standard being recorded. For example, for recordings such as CD-digital audio recordings, the track matching requirements may be accomplished with little more than a deliberate gap left at the point where the tracks formed by two adjacent heads meet. In effect that approach mimics a scratch on the medium. In cases where greater precision is required, it is possible to interrupt the write operation of HEAD 2 for example as it approaches its end point (which is also the point where HEAD 1 began to write). At that point, the coarse positioning actuator can be disabled in order to minimize interference from that source and the final gap measured relative to the encoder disc 20. This gap can be measured more precisely by using a circuit which produces multiples of the basic pseudoclock signal sufficient to meet the measurement requirements of the recording standard being employed. HEAD 3 can then be redirected to where it left off and can continue writing. A circuit which employs the higher frequency pseudoclock as a reference then selects a strategy whereby the difference between the two points are measured by these triggering edges and the circuit adjusts the one to the other in small, non-disruptive increments.

Such a configuration presents a subtly different range of requirements than does a READ-ONLY system.

The outermost WRITE HEAD encounters the highest linear track velocity for a given angular velocity and hence the outermost head must deliver the highest rate of write pulses. Since the write pulse/marking characteristics impose significant increases in costs for each increase in laser power, control electronics speed, etc., it is most practical to specify that the outermost head should operate at the design limits of the system. That is, the outermost head should have the fastest operating rate and, optimally the spindle control should maintain a constant linear velocity consistent with that maximum so that the system operates at its specified maximum data rate at all times.

For example, if the outermost head operates at a constant linear velocity which is 4 times normal CLV, each of the other heads will record its assigned data area at a rate which is slower than the outermost head depending on its relative radial position (eg., the innermost head will operate at less than half the data rate of the outermost head).

Parallel operation of multiple heads also requires either an interleaved single data stream or appropriately proportioned parallel data streams. In sum, data destined to each of the different heads will be interleaved so that data frames can be fed to each head at appropriate rates which more or less match the local data rate at each head. As such interleaving rates are functions of the relative radial position of each head the interleave ratios can be readily determined by, for example, monitoring the addresses recovered from the track 29. In some circumstances it is desirable that the data to be recorded should be stored on a system which can in fact deliver appropriately interleaved data.

The write data buffer associated with each head must be capable of reclocking data from input lines recovered from a network or satellite operating at a single clock rate. It must then be clocked out of the buffer at the pseudoclock rates determined by the track 29 at a location corresponding to that head. Each head will require its own data strobe/buffer interface.

Such a system, especially one serving to record data delivered over a network, inevitably encounters communications losses, interruptions, etc. Consequently, such systems should make provision for a high speed buffering capacity which is scaled to serve the requirements of each head and its unique data rate. In order to minimize buffer capacities it is possible to institute a technique which delays the writing of tracks as required in the manner proposed for read-only devices, above.

WRITE operations on contemporary media are by and large a function of energy delivered to a given track area in a given time. There are a number of nuances involved, most particularly the lateral transmission of energy through the recording film and vertically between composite media layers including the substrate. As a consequence, the most satisfactory WRITE-PULSE control configurations make provision for specific shaping of the WRITE-PULSE pattern such as an increased power output from the laser at the beginning of any individual pit formation operation in order to overcome (largely lateral) transmission losses and deliver sufficient energy to produce appropriate leading edges while the following portions of each mark are generally formed by lower power pulses because pulses delivered immediately prior will contribute a "pre-warming" component through transmission. This is typically referred to as a "WRITE-PULSE shaping circuit". Such a circuit must make provision to compensate for any differential cooling rate which occurs as a result of the lower linear velocity encountered by the inner, (i.e. slower),

heads and in some configurations such compensation may include modulating the secondary WRITE-PULSE form.

The multiple heads provided on the drive also permits simultaneous operation of writing of data and reading of data for verification. Considering, for example, the embodiment shown in Figure 1, the head 33a may be utilized to write data to the data carrier 12 and the diametrically opposed head 33c may be used to read the data recorded by the head 33a and verify the accuracy of the recorded data. The data will be readable by the head 33c as it derives the appropriate clock circuit from the track 29. Such an arrangement is particularly beneficial for archival backup. The provision of the encoding disc 20 permits the archival recordal to be interrupted and for the data position to be recovered with the appropriate timing when archival recording is reinstated.

The ability to radially position the heads independently may also be used to enhance the maximum data transfer rate as shown in Figure 10. A wide divergence of the heads - that is, place of the heads at radially disparate locations - will restrict the data rate retrieved from one of those heads. One head will be operating at a maximum rate while the other is operating at below optimum.

As shown in Figure 10, when writing date to the carrier 12, each of the heads 33 is located in one of a number of sectors on the disc surface. Thus, rather than positioning the four heads equidistant across the radius of the data carrier, the heads are grouped together in a relatively narrow band and data is provided to the heads as described above to record respective areas of the data carrier. Because the heads are grouped closely together, the disparity between the maximum and minimum rates of the head is reduced and the overall data rate of recordal is enhanced. Once the data has been written to the sector, the heads are repositioned and realigned as described above, and the next sector written. This is repeated sector by sector until the recording is complete.

With such an arrangement, upon completion of recording of each sector, the heads may be switched from a WRITE to a READ mode and continue to read the data previously recorded by the adjacent head. The radially outer head is repositioned at the radially inner track of the sector just recorded so that each portion of the sector is verified. Again, this arrangement permits writing and verification at the maximum data rate of each of the heads and may proceed on a sector-by-sector basis until the recording is complete. The control and coordination of the various subsystems described above is accomplished

with the use of a dedicated microprocessor. Each of the head assemblies 33 is controlled by a separate microprocessor which may be self-programmed at startup by the controlling microprocessor. The separate microprocessors in each of the heads control positioning, data timing and fine control of the WRITE pulse. It will be understood that such operational controls could be configured in a number of ways known in the prior art. Although the nature of the control software will depend upon the particular application and strategies to be employed, an example of the control effected by the microprocessor is set out below as a sequence of control steps upon initiation. It is assumed for the purpose of description that a pair of head assemblies are used, although it will be appreciated that similar sequences are implemented where more than two heads are utilized with appropriate modification to the command structure.

In some configurations of very high speed writing, it may be necessary to employ circuits which closely control the relative power of the WARMING and WRITE pulses and it is possible that such a circuit may be required to differentiate between the writing of short and long marks due to the impact of the outer portions of the laser spot extending into the area of the next mark to be written. Automatic circuitry to maintain such control is implemented in a microprocesser utilizing known control sequences is discussed below.

A READ-ONLY SEQUENCE proceeds as follows:

1. OPERATOR SELECTS READ-ONLY MODE
2. START-UP ALIGNMENT SEQUENCE ON ENCODER DISC 20
    2.1 CONTROLLER CIRCUIT SETS INITIAL STATES
    2.1.1 PSEUDOCLOCK RECOVERY CIRCUITS - DISABLED

        SET BOTH PHASE-LOCKED
        LOOP/VOLTAGE CONTROLLED
        OSCILLATOR(PLL/VCO) CENTER
        FREQUENCIES FOR 4 RPS
        ACTION: SELECTS REQUIRED
        RESISTOR IN VCO LOOP

2.1.2 FINE TRACKING ACTUATOR - FOUR CIRCUITS DISABLED

2.1.3 FINE FOCUS ACTUATORS:

ENCODER DISC 20 HEAD #1 - ENABLED
ENCODER DISC 20 HEAD #2 - ENABLED
READ/WRITE HEAD #1 - DISABLED
READ/WRITE HEAD #2 - DISABLED

2.1.4 ADDRESS RECOVERY CIRCUITS - DISABLED

2.2 CONTROLLER CIRCUIT COMMANDS

2.2.1 TO TURNTABLE CONTROL CIRCUIT - SPIN AT 4 RPS
2.2.2 TO COARSE POSITIONING CIRCUIT

THE CONTROLLER CIRCUIT TAKES DIRECT CONTROL OF THE STEPPER MOTOR, MAKING THE STAGE MOVE OUTWARD ALONG THE RADIUS

2.2.3 CONTROLLER CIRCUIT RECEIVES A SIGNAL FROM MICROSWITCH #1 INDICATING STAGE IS AT THE PROPER RADIUS TO READ ALIGNMENT TRACKS.
2.2.4 CONTROLLER CIRCUIT STOPS THE STEPPER MOTOR.

2.3 CONTROLLER CIRCUIT SETS NEW FOCUS & TRACKING STATES

2.3.1 FINE FOCUS CIRCUITS - ALL 4 ENABLED
2.3.2 FINE TRACKING CIRCUITS - ALL 4 ENABLED

FOCUS AND TRACKING CIRCUITS OPERATE AUTOMATICALLY

2.4 CONTROLLER CIRCUIT CHECKS FOR STATUS

2.4.1 FROM FINE FOCUS CIRCUIT - "FOCUS OK"

2.4.2 FROM FINE TRACKING CIRCUIT - "TRACKING OK"

AFTER RECEIPT OF BOTH SIGNALS FROM ALL FOUR HEADS

2.5 CONTROLLER CIRCUIT TO PSEUDOCLOCK RECOVERY CIRCUIT

- PSEUDOCLOCK RECOVERY PLL CIRCUIT - ENABLED

2.6 CONTROLLER CIRCUIT CHECKS STATUS

2.6.1 FROM ALL 4 PSEUDOCLOCK PLL - "PHASELOCK OK"

2.7 CONTROLLER CIRCUIT SETS ADDRESS RECOVERY STATUS

2.7.1 ADDRESS RECOVERY CIRCUITS- ALL 4 ENABLED

2.8 CONTROLLER CIRCUIT CO-ORDINATES:
ADDRESS RECOVERY & PSEUDOCLOCK RECOVERY CIRCUITS

2.8.1 CONTROLLER CIRCUIT DETECTS FRAME PULSES
SOURCES: PSEUDOCLOCK RECOVERY CIRCUITS
REQUIREMENT: TWO RUNNING COUNTS

2.8.2 CONTROLLER CIRCUIT COUNTS PSEUDOCLOCK PULSES
SOURCES: PSEUDOCLOCK RECOVERY CIRCUITS

REQUIREMENT: COUNT THE 588 PSEUDOCLOCK (OR, CHANNEL BIT) PULSES FROM EACH HEAD WHICH CORRESPOND TO THE SEPARATION BETWEEN 2 FRAME PULSES.

2.8.3 THE CONTROLLER CIRCUIT READS ADDRESSES FROM THE ADDRESS RECOVERY CIRCUITS

CONTROLLER CIRCUIT CO-ORDINATES THE ADDRESS FOR EACH OF THE 4 HEADS WITH ITS FRAME PULSE COUNT AND CHANNEL BIT COUNT IN ORDER TO DETERMINE THE CURRENT POSITION OF EACH OPTICAL HEAD TO A ONE CHANNEL BIT TOLERANCE OR BETTER.

2.9 CONTROLLER CIRCUIT SETS TRACKING OFFSETS
CONTROLLER CIRCUIT COMPARES ADDRESSES FROM EACH HEAD PAIR AS THEY READ THE ALIGNMENT TRACKS AND DETERMINES WHETHER THE ENCODER DISC 20 AND READ/WRITE HEADS ARE SET AT APPROPRIATE RADIAL OFFSETS.

2.9.1 IF YES - NO OFFSET

2.9.2 IF NO - CONTROLLER CIRCUIT SENDS + OR - TRACK JUMP PULSES TO THE ENCODER DISC 20 FINE TRACKING ACTUATOR ON EACH PAIR UNTIL THE HEADS ARE ADDRESSING THE CORRECT OFFSET FRAMES.

ONCE HEADS ARE AT CORRECT OFFSET, THE CONTROLLER CIRCUIT MEASURES THE DC OFFSET BETWEEN THE HEADS BY SAMPLING THE SIGNAL FROM THE HEAD POSITION SENSOR

CONTROLLER CIRCUIT SETS A DC OFFSET FOR THE FINE TRACKING CIRCUIT OF THE ENCODER DISC 20 HEAD

2.10 CONTROLLER CIRCUIT CHECKS RADIAL ALIGNMENT
CONTROLLER CIRCUIT SAMPLES THE DATA STREAMS FROM THE TWO OFFSET TRACKS TO DETERMINE THE RELATIVE

RADIAL MISALIGNMENT OF THE OFFSET HEADS

2.10.1 OPERATION WITHIN ACCEPTABLE TOLERANCES

IF THE HEADS ARE ALIGNED TO THE RADIUS WITHIN ACCEPTABLE TOLERANCES, THE CONTROLLER CIRCUIT WILL COMPENSATE FOR MISALIGNMENT BY PSEUDOCLOCK OFFSETS

2.10.2 OPERATION IF BEYOND ACCEPTABLE TOLERANCES IF THE HEADS ARE NOT ACCEPTABLY ALIGNED TO THE RADIUS, THE CONTROLLER CIRCUIT WILL PAUSE AND SIGNAL THE OPERATOR TO ADJUST RADIAL ALIGNMENT USING THE MICROMETER RADIAL ADJUSTMENT ON EACH STAGE

NB: ACCEPTABLE ALIGNMENT WILL BE SPECIFIED AS A FUNCTION OF PSEUDOCLOCK CYCLES AFTER TESTING OF THE SYSTEM

3. ALIGN TO TARGET DISC

NOW THE READ/WRITE HEADS HAVE TO BE ALIGNED TO THE TARGET DISC SO THEY CAN BE ACCURATELY POSITIONED

3.1 CONTROLLER CIRCUIT SETS TARGET ALIGNMENT INITIAL STATES

3.1.1 PSEUDOCLOCK RECOVERY CIRCUITS - DISABLED

BOTH PLL/VCO CENTER FREQUENCIES REMAIN SET FOR 4 RPS

3.1.2 FINE TRACKING ACTUATOR - 4 CIRCUITS DISABLED

3.1.3 FINE FOCUS ACTUATORS:

ENCODER DISC 20 HEAD #1 - ENABLED

ENCODER DISC 20 HEAD #2 - ENABLED

READ/WRITE HEAD #1 - DISABLED

READ/WRITE HEAD #2 - DISABLED

3.1.4 ADDRESS RECOVERY CIRCUITS - DISABLED

3.2 CONTROLLER CIRCUIT COMMANDS

3.2.1 TO TURNTABLE CONTROL CIRCUIT - SPIN AT 4 RPS

3.2.2 TO COARSE POSITIONING CIRCUIT - THE CONTROLLER CIRCUIT TAKES DIRECT CONTROL OF THE STEPPER MOTOR, MAKING THE STAGE MOVE INWARD ALONG THE RADIUS

3.2.3 CONTROLLER CIRCUIT RECEIVES A SIGNAL FROM MICROSWITCH #2 INDICATING STAGE IS AT THE PROPER RADIUS TO ALIGN WITH THE TARGET DISC

3.2.4 CONTROLLER CIRCUIT STOPS THE STEPPER MOTOR

3.3 CONTROLLER CIRCUIT SETS NEW FOCUS & TRACKING STATES

3.3.1 FINE FOCUS CIRCUITS - ALL 4 ENABLED

3.3.2 FINE TRACKING CIRCUITS - ALL 4 ENABLED

FOCUS AND TRACKING CIRCUITS OPERATE AUTOMATICALLY

3.4 CONTROLLER CIRCUIT CHECKS FOR STATUS

3.4.1 FROM FINE FOCUS CIRCUIT - "FOCUS OK"

3.4.2 FROM FINE TRACKING CIRCUIT - "TRACKING OK"

AFTER RECEIPT OF BOTH SIGNALS

3.5 CONTROLLER CIRCUIT TO PSEUDOCLOCK RECOVERY CIRCUIT

PSEUDOCLOCK RECOVERY CIRCUITS - ENABLED

3.6 CONTROLLER CIRCUIT CHECKS STATUS

3.6.1 FROM PSEUDOCLOCK CIRCUITS - "PHASELOCK OK"

3.7 CONTROLLER CIRCUIT SETS ADDRESS RECOVERY STATUS

3.7.1 ADDRESS RECOVERY CIRCUIT - ENABLED

3.8 CONTROLLER CIRCUIT CO-ORDINATES: ADDRESS RECOVERY & PSEUDOCLOCK RECOVERY CIRCUITS

3.8.1 CONTROLLER CIRCUIT DETECTS FRAME PULSES
SOURCES: PSEUDOCLOCK RECOVERY CIRCUITS
REQUIREMENT: TWO RUNNING COUNTS

3.8.2 CONTROLLER CIRCUIT COUNTS PSEUDOCLOCK PULSES
SOURCES: PSEUDOCLOCK RECOVERY CIRCUITS
REQUIREMENT: COUNT THE 588 PSEUDOCLOCK (OR, CHANNEL BIT) PULSES BETWEEN 2 FRAME PULSES FROM EACH HEAD.

3.8.3 CONTROLLER CIRCUIT READS ENCODER DISC 20 ADDRESSES FROM THE TWO ENCODER DISC 20 ADDRESS RECOVERY CIRCUITS

3.8.4 CONTROLLER CIRCUIT READS TRACKING DATA FROM THE FINE TRACKING CIRCUITS ASSOCIATED WITH BOTH READ/WRITE HEADS TO DETERMINE THE POINT WHERE THE TRACK RUNS OUT
NB: DURING READ OPERATIONS THERE MAY BE EITHER DATA PITS IN GROOVES, OR, ONLY PRE-GROOVED WOBBLE TRACKS WITHOUT DATA ON THE TARGET DISC. WE HAVE OPTED TO WORK WITH TRACKING DATA FROM THE GROOVES BECAUSE GROOVES WILL BE THERE IN EITHER CASE
ACTION: READ/WRITE & ENCODER DISC 20 HEAD PAIRS TRACK AUTOMATICALLY TO TRACK-END
(i.e. The end of the target disc's groove or track)

3.8.5 CONTROLLER CIRCUIT IDENTIFIES ENCODER DISC 20 ADDRESS FOR EACH READ/WRITE HEAD AT TRACK END

3.8.6 CONTROLLER CIRCUIT CONFIRMS THAT RADIAL OFFSET IS ACCEPTABLE BY REFERENCE TO POSITION SENSORS. THIS WILL REQUIRE PEAK-HOLD/BOTTOM-HOLD SAMPLING OF THE DATA FROM THE POSITION SENSORS ON THE READ/WRITE HEADS TO GET A SIGNAL WHICH ALLOWS FOR THE ECCENTRICITY OF THE TARGET DISC

ONCE THE OFFSET POSITION HAS BEEN CONFIRMED:

3.9 CONTROLLER CIRCUIT CHANGES STATUS

3.9.1 ENCODER DISC 20 PSEUDOCLOCK RECOVERY - DISABLED

3.9.2 ADDRESS RECOVERY CIRCUITS - DISABLED

3.10 CONTROLLER CIRCUIT SENDS TRACK JUMP PULSE COMMANDS TO THE FINE TRACKING CIRCUITS OF EACH PAIR OF HEADS

3.10.1 IN RESPONSE TO JUMP PULSE COMMANDS, FINE TRACKING CIRCUITS INJECT TRACK JUMP PULSES DIRECTLY TO THE FINE POSITION ACTUATORS OF BOTH HEADS IN EACH PAIR CAUSING THEM TO JUMP INWARD ONE TRACK PER PULSE.

3.10.2 CONTROLLER CIRCUIT COUNTS TRACK JUMPS UNTIL DESIRED RADIAL LOCATION IS REACHED FOR EACH HEAD

3.11 CONTROLLER CIRCUIT CHANGES STATUS

3.11.1 PSEUDOCLOCK RECOVERY CIRCUITS - ENABLED

3.12 CONTROLLER CIRCUIT CHECKS PHASE TO CHANGE STATUS

3.12.1 CONTROLLER CIRCUIT CHECKS OUTERMOST PSEUDOCLOCK RECOVERY CIRCUIT FOR "PHASELOCK OK"

3.12.2 ADDRESS RECOVERY CIRCUIT - ENABLED

3.13 CONTROLLER CIRCUIT INITIATES CONSTANT LINEAR VELOCITY (CLV) OPERATION

3.13.1 TURNTABLE CONTROL CIRCUIT -SWITCHED

THE SYSTEM BEGINS TO OPERATE ON CLV CONTROLLED BY THE OUTERMOST HEAD PAIR

ACTION: THE TURNTABLE CONTROL CIRCUIT'S REFERENCE IS CHANGED FROM THE ROTARY ENCODER TO THE COMPARISON CIRCUIT WHICH USES A PHASE-LOCKED LOOP TO COMPARE THE PSEUDOCLOCK PULSE RATE (RECOVERED FROM THE ENCODER DISC 20 HEAD ASSOCIATED WITH THE OUTERMOST HEAD PAIR) WITH A 4.3218 MHz CLOCK

3.14 CONTROLLER CIRCUIT CHECKS PHASE BEFORE CHANGING STATUS ON INNERMOST HEAD PAIR:

3.14.1 CONTROLLER CIRCUIT CHECKS THE INNERMOST HEAD PAIR'S PSEUDOCLOCK RECOVERY CIRCUIT FOR "PHASELOCK OK"

3.14.2 ADDRESS RECOVERY CIRCUIT - ENABLED

4. READ ENABLED FOR BOTH HEADS

4.1 SIGNALS FROM BOTH HEADS IN THE OUTERMOST (CLV) HEAD PAIR ARE SENT TO THE OSCILLOSCOPE FOR COMPARISON

4.2 SIGNALS FROM BOTH HEADS IN THE INNERMOST (OFFSET) HEAD PAIR ARE SENT TO THE OSCILLOSCOPE FOR COMPARISON

WRITE OPERATION SEQUENCE: OPERATOR SELECTS WRITE MODE NOTE: WRITE FUNCTIONS ARE IDENTICAL TO READ FUNCTIONS FOR ALL OF THE STEPS DETAILED IN SECTIONS 2 AND 3

5. CONTROLLER CIRCUIT SETS WRITE ENABLED STATUS FOR BOTH HEADS

5.1 CONTROLLER CIRCUIT READS ADDRESSES FROM ENCODER DISC 20 ADDRESS RECOVERY CIRCUIT FOR THE OUTERMOST (CLV) HEAD PAIR. CONTROLLER CIRCUIT SETS "WRITE ENABLED" STATUS FOR WRITE PULSE CIRCUIT AT SELECTED ADDRESS.

SPECIFIED RADII FOR CLV WRITE: 53 mm to 58 mm

5.2 CONTROLLER CIRCUIT READS ADDRESSES FROM ENCODER DISC 20 ADDRESS RECOVERY CIRCUIT FOR THE INNERMOST (CLV) HEAD PAIR. CONTROLLER CIRCUIT SETS "WRITE ENABLED" STATUS FOR WRITE PULSE CIRCUIT AT SELECTED ADDRESS

SPECIFIED RADII FOR OFFSET WRITE: 21.7 mm TO 29.7 mm

6. WRITE PULSE CIRCUITS OPERATE

ONCE ENABLED THE WRITE PULSE CIRCUITS REFER TO THE PSEUDOCLOCK PULSE IN ORDER TO MAKE DESIGNATED MARKS WHICH ARE MULTIPLES OF THE PSEUDOCLOCK PULSE. (EG. "I-3'S"

COMPOSED OF 3 CLOCK PULSES FOR ONE HEAD AND "I-6'S" FOR THE OTHER HEAD.) PATTERNS CAN BE SELECTED IN ADVANCE OR CAN BE PROGRAMMABLE

7. CONTROLLER CIRCUIT DISABLES WRITE STATUS FOR BOTH HEADS
   7.1 CONTROLLER CIRCUIT READS ADDRESSES FROM ENCODER DISC 20 ADDRESS RECOVERY CIRCUIT FOR THE OUTERMOST (CLV) HEAD PAIR. CONTROLLER CIRCUIT SETS "WRITE DISABLED" STATUS FOR WRITE PULSE CIRCUIT AT SELECTED ADDRESS
   7.2 CONTROLLER CIRCUIT READS ADDRESSES FROM ENCODER DISC 20 ADDRESS RECOVERY CIRCUIT FOR THE INNERMOST (CLV) HEAD PAIR. CONTROLLER CIRCUIT SETS "WRITE DISABLED" STATUS FOR WRITE PULSE CIRCUIT AT SELECTED ADDRESS

8. CONTROLLER CIRCUIT PAUSES ALL SYSTEMS AND MAINTAINS RADIUS WAITING FOR INSTRUCTIONS

READ AFTER WRITE OPERATION

1. OPERATOR SELECTS READ-AFTER-WRITE MODE
2. CONTROLLER CIRCUIT REPOSITIONS BOTH HEAD PAIRS TO THE SAME RADII
   2.1 CONTROLLER CIRCUIT MAINTAINS STATUS
      2.1.1 FINE FOCUS - ENABLED
      2.1.2 FINE TRACKING - ENABLED
      2.1.3 PSEUDOCLOCK RECOVERY - ENABLED
      2.1.4 ADDRESS RECOVERY - ENABLED

•

NB: THE TEST RECORDING SEQUENCES MAY BE SHORT ENOUGH THAT PSEUDOCLOCK RECOVERY AND ADDRESS RECOVERY MAY

NOT HAVE TO BE DISABLED AND ENABLED AS IN EARLIER SEQUENCES. ALTERNATIVELY, WE MAY IMPLEMENT THE ADDRESS RECOVERY CIRCUIT SO THAT THE "PHASELOCK OK" SIGNAL FROM THE PSEUDOCLOCK RECOVERY CIRCUIT ENABLES THE ADDRESS RECOVERY CIRCUIT

2.2 CONTROLLER CIRCUIT READS ADDRESS RECOVERY

2.3 CONTROLLER CIRCUIT ENABLES READ FUNCTIONS ON BOTH HEADS AT CORRECT ADDRESSES. SAME FUNCTION AS IN READ-ONLY OPERATION

TRACK CONTINUITY SEQUENCE

1. OPERATOR SELECTS TRACK CONTINUITY MODE CONTROLLER CIRCUIT CONDUCTS OPERATIONS AS WITH READ MODE AND WRITE/READ-AFTER-WRITE MODE WITH THE FOLLOWING EXCEPTIONS:

2. CONTROLLER CIRCUIT SETS PSEUDOCLOCK PLL/VCO CENTER FREQUENCY TO APPROPRIATE RANGE

3. CONTROLLER SELECTS TARGET TRACK MEETING ADDRESS

3.1 CONTROLLER CIRCUIT DIRECTS OUTERMOST HEAD TO TARGET RADIUS, READS ADDRESSES AND INITIATES WRITE OPERATION AT Appropriate ADDRESS

SPECIFIED RADII FOR CLV WRITE: 56 mm to 61 mm

SPECIFIED PIT PATTERN: I-6 (6 clock cycles)

3.2 CONTROLLER CIRCUIT DIRECTS INNERMOST HEAD TO SAME TARGET RADIUS AS OUTERMOST HEAD

3.2.1 CONTROLLER CIRCUIT READS ADDRESSES TO CONFIRM LOCATION.

3.2.2 CONTROLLER CIRCUIT COMPARES ALIGNMENT TO ENCODER DISC 20 ADDRESS GIVEN TO OUTERMOST

HEAD

NB: AT THIS POINT THE INNERMOST HEAD IS ASSIGNED TO READ THE TRACK WHICH THE OUTERMOST HEAD HAS JUST WRITTEN IN ORDER TO CONFIRM ALIGNMENT SO CONTINUOUS TRACKS CAN BE WRITTEN

3.2.3 CONTROLLER CIRCUIT ADJUSTS CLOCK OFFSET SO TRACKS CREATED BY INNERMOST HEAD PAIR WILL MEET THE TRACK JUST WRITTEN BY OUTERMOST HEAD APPROPRIATELY

3.3 CONTROLLER CIRCUIT DIRECTS INNERMOST HEAD TO ITS START WRITE RADIUS

SPECIFIED RADII FOR OFFSET WRITE: 51 mm to 56 mm

SPECIFIED PIT PATTERN: I-3 (3 clock cycles)

3.4 CONTROLLER CIRCUIT READS INNERMOST ADDRESSES AND INITIATES WRITE OPERATION AT APPROPRIATE ADDRESS

3.5 CONTROLLER CIRCUIT DISABLES OUTERMOST (CLV) WRITE PROCESS AT APPROPRIATE ADDRESS

3.6 CONTROLLER CIRCUIT DISABLES INNERMOST (OFFSET) WRITE PROCESS AT A POINT WHICH IS 20 PSEUDOCLOCK CYCLES BEFORE THE START-WRITE ADDRESS FOR THE OUTERMOST CLV HEAD

4. CONTROLLER CIRCUIT PAUSES OPERATIONS CONFIRM - CONTINUITY READ

1. OPERATOR SELECTS CONFIRM CONTINUITY MODE

2. CONTROLLER CIRCUIT SETS STATUS

2.1 INNERMOST HEAD: ALL SYSTEMS DISABLED

2.2 OUTERMOST HEAD: CLV READ MODE

2.2.1 CONTROLLER CIRCUIT DIRECTS HEAD TO TARGET RADIUS

SPECIFIED OPERATING RADII: 53 mm to 58 mm

2.3 CONTROLLER CIRCUIT DIRECTS TURNTABLE CONTROL CIRCUIT TO SPIN UNDER CLV CONTROL

2.4 FINE FOCUS - ENABLED

2.5 FINE TRACKING - ENABLED

2.6 PSEUDOCLOCK RECOVERY - ENABLED

2.7 ADDRESS RECOVERY - ENABLED

3. CONTROLLER CIRCUIT READS ADDRESSES AND ENABLES READ OPERATIONS SO THE TWO TRACK PIT PATTERNS CAN BE READ.

3.1 CONTROLLER CIRCUIT READS AND DISPLAYS ADDRESS FOR INNERMOST TRACK END

3.2 CONTROLLER CIRCUIT READS AND DISPLAYS ADDRESS FOR OUTERMOST TRACK END

3.3 CONTROLLER CIRCUIT DISPLAYS THE SEPARATION BETWEEN TRACKS AS A NUMBER OF CLOCK CYCLES

4. CONTROLLER CIRCUIT PAUSES SYSTEM SO CONFIRMATION READ CAN BE DONE AGAIN OR THE SYSTEM CAN BE SHUT DOWN

SHUT DOWN MODE

1. OPERATOR SELECTS SHUTDOWN
2. CONTROLLER CIRCUIT TAKES DIRECT CONTROL OF COARSE POSITIONING MOTORS AND MOVES BOTH STAGES OUTWARD ALONG THE RADIUS UNTIL THE SIGNAL IS RECEIVED FROM MICROSWITCH # 1 INDICATING THAT THE SHUTDOWN POSITION HAS BEEN REACHED
3. OPERATOR SHUTS DOWN THE SYSTEM.

It will be noted that these sequences are somewhat simplified for the purposes of this application and that many variations are possible using alternate mechanical, electromechanical, electronic, optical, and opto-electronic components. many

of which are listed or referred to in the foregoing disclosure.

In the above embodiment, the timing signal has been retrieved from the encoded disc that is concentrically located about the carrier 12. An alternative arrangement is shown in Figure 11, in which the encoder disc 20 is located below the carrier 12. As shown in Figure 11, the radial extent of the encoding disc 20 and the data carrier is the same so that a CLV-like pattern may be used on the encoding disc. Each of the heads 34,36 is radially aligned and directed in opposite direction so that head 34 derives the timing signal from the encoding disc 20. The data format for the encoding disc described above may of course be utilized to provide the requisite accuracy. It should be noted that other zero-sum code patterns may be desirable for use with encoder discs which do not employ a radial offset and so require different scales to assure scanning at I-top.

As an alternative to the frequency multiplier utilized to accommodate the two different scan rates for CLV, an alternative arrangement is shown in Figure 12. In this arrangement, the encoding disc 20b is formed with two layers 120,122. The layer 120 carries the encoding pattern for one of the standards and the layer 122 carries the encoding pattern for the other of the standards. The head 34 is provided with a differential focus so that it can be switched between the two layers 120,122 and thereby read the timing pattern associated with the appropriate standard.

A further enhancement of the synchronization of the timing pattern provided by the track 29 may be obtained by utilizing the relationship between adjacent passes of the track. Each of the passes contains marks which are approximately ten clock cycles longer than the preceding rotation. Accordingly, the timing pattern may be adjusted by redirecting the scanning spot on the track 29 in or out in single track increments to effect a fine-tuning of the recovered frequency to that at which the disc was recorded. This method of measuring data pit lengths on the carrier 12 appears to be superior to the conventional approach about these two orders of magnitude.

In the preferred embodiments described above, a separate encoder disc is utilized to generate the timing pattern. While the use of a separate track is considered most desirable and offers optimum accuracy, it will be recognized that a clock signal may be derived from the data recorded directly on the carrier 12. For READ-only operation, it is possible to employ conventional means other than the encoder-based system noted above to stabilize the channel bit frequency provided electronic circuits of sufficient speed are

employed. Specifically, the frequency can be maintained with sufficient stability by comparing the frequency recovered from the data track of a recorded disc to the frequency of a fast system clock numerically while making provision for a count of each and allowing for the increase in frequency which will occur as the head transits outward. A circuit derives a numerical measure of the rotation rate and the frequency recovered can be compared numerically to a frequency reference value stored in a look-up table with reference to the absolute track address recorded in subcode. This requires that the primary modulation rate - either 1.2 or 1.4 m/s - is factored into the equation.

Similarly, the relative clock rate may be calculated as a function of the number of the spiral, i.e. radial location, employing the incremental change in track length between mutually adjacent tracks, again allowing for the primary modulation rate. Alternatively, some combination of the synchronizing marks (which are separated by 588 clock cycles corresponding to 588 channel bits) may be compared to a frequency produced in the manner of a sampled servo using the intervals between subcode addresses and either or both frequencies may be phase locked to the pit/edge transitions which record the data.

A further technique for retrieving a clock signal is to rely upon the tolerances found in typical discs in the CD system which can be formed with a basic clock rate that varies +/- 1% from the precise standard specified. The variation produces a deviation from a fixed clock rate which is referred to as the "jitter margin" and which is normally solved by a buffer structure. The track 29 provides a superior solution. Specifically, as a result of the relation between a spiral and CLV operation, each track contains marks which are approximately 10 clock cycles longer than the preceding track. Incorporation of a track-offset circuit capable of redirecting the scanning spot on the track 29 in or out in single track increments will, in effect, fine-tune the pseudoclock frequency to that at which the disc was recorded. This method of measuring data pit lengths on the target disc is superior to the conventional approach by at least two orders of magnitude.

The recovery of the clock signal may employ elements of the sampled servo approach discussed above, the detection of ATIP mark from a CDR disc, for example, or by simple use of the synchronization pulses embedded in the data of a conventional CD or other such disc. Logic circuits can be employed to determine whether the relative clock rates are changing in an incremental fashion which exceeds the specified tolerance. Such a determination will then be used to control a pseudoclock compensation circuit in both

WRITE and READ-ONLY applications. Where an encoding disc is utilized. then the detected variations can be made to compensate for differences between the spatial pattern encoded on the disc and the patent formed on the carrier 12.

The clock timing may be recovered by a combination of the above techniques such as in one embodiment the provision of an ATIP sampled servo pattern and address extraction circuitry that can recover the ATIP addresses. Alternatively, the ATIP addresses can be included with a sample servo circuit that may provide additional reference to control for eccentricity, etc. As a further alternative, a pre-formatted disc may be utilized for recording which incorporates a wobble track pattern as well as the sample servo mark such as the ATIP marks which provide the requisite clock accuracy. Where it is desirable to record on a featureless flat carrier without a pregroove, the provision of the encoder disc 20 permits control of the clocking as the radial position of the heads is adjusted by monitoring the track previously written by means of a side spot formed by placing a defraction grating in the optical path of the head. In this way, the spacing from the previously recorded track can be maintained constant using detection circuits similar to a three-beam optical tracking system.

For record operations, optical heads should make provision for incorporation of a lens position sensor and read-out circuit which signal can be used for coordination of fine lens positioning between the READ and WRITE heads and as a control parameter for a course positioner and as a secondary positional reference for offset track location. Alternatively, lens position sensors may be developed to be retrofitted to conventional READ heads or circuits can be employed which measure lens position by reference to the fine tracking error drive signal.

SECOND PREFERRED EMBODIMENT

In this approach, the same system is employed with the exception that the pre-formatted recordable disc employs a sampled servo pattern, such as ATIP, and the drive contains circuitry capable of recovering the ATIP addresses. This embodiment permits the recovered ATIP addresses to be employed for the verification of track positioning by the kick track circuit.

THIRD PREFERRED EMBODIMENT

In this approach, the same system is employed as in the second embodiment but with provision for the inclusion of a sample servo circuit which may provide additional reference to control for eccentricity, etc. as well as recovering the ATIP addresses. This embodiment also permits the recovered ATIP addresses to be employed for the verification of track positioning by the kick track circuit.

FOURTH PREFERRED EMBODIMENT

In this approach, no displaced encoder is employed and the preformatted disc incorporates a wobble track pattern (or comparable contrasting timing pattern) as well as sufficient sampled servo marks such as ATIP marks which are sufficient to effectively replace the offset or otherwise displaced encoder.

In effect, all four embodiments are comparable because all of them employ an encoder timing track disc with or data format as a track measurement device and also as a scannable pattern for the production of a pseudoclock signal suitably precise to control multiple head writing and reading.

However, it is possible that the present invention may incorporate a radial tracking system which enables it to record on featureless flat target discs making more extensive use of the STOL reference in combination with the detection of the adjacent track just written by a side spot formed by placing a diffraction grating in the optical path of the head which operation is possible using a device similar to a 3-beam optical tracking means with provision for electronic circuitry to compare signals retrieved from position sensors incorporated into the offset heads with the tracking signal received from a single side of the 3-beam tracking optics.

For record operations, optical heads should make provision for incorporation of a lens position sensor and read out circuit which signal can be used for co-ordination of fine lens positioning between the READ and WRITE heads and as a control parameter for the coarse positioner and as a secondary positional reference for offset track location. Alternatively, lens position sensors may be developed to be retrofitted to conventional read heads or circuits can be employed which measure lens position by reference to the fine tracking error drive signal.

It should be noted that the depiction of linked head assemblies is for illustration purposes only and that each head in a pair may be mounted on a separate stage and aligned electronic offset by reference to minimal address data on either a preformatted CD-R disc or to the data subcode on a recorded disc such that an approach may be preferable in that it reduces physical alignment requirements for the radial translation stages which position the heads and thus simplifies fabrication of the drive.

Of course, while operation of the head assemblies has been described as read or record, it will be appreciated that the head assemblies may operate independently so that one may record while another verifies and the balance read data.

WHAT IS CLAIMED IS:

1. An optical drive to transfer data between a data carrier and a data communication circuit, said drive having a support to rotate said carrier about an axis and having a plurality of optical head assemblies disposed about said axis, each of said head assemblies being radially adjustable relative to said axis to scan said carrier as it rotates and each of said head assemblies having a clock recovery circuit associated therewith to obtain a clock signal for data processed by respective ones of said optical head assemblies whereby a plurality of data streams may be processed.

2. An optical drive according to claim 1 wherein one of said clock signals is utilized to control rotation of said carrier and maintain said one clock signal at a predetermined frequency.

3. An optical drive according to claim 2 wherein clock signals associated with each of said head assemblies are compared to a reference signal and said one signal selected based on such comparison.

4. An optical drive according to claim 2 wherein said one clock signal is selected by comparing address information indicative of the relative radial locations of said head assemblies.

5. An optical drive according to claim 2 wherein address information indicative of the relative positions of said head assemblies is monitored and a corresponding rotational speed dervied therefrom from data stored in a look-up table.

6. An optical drive according to claim 1 wherein said clock signals are derived from a timing track conjointly rotatable with said carrier and providing a clock signal correlated to the radial position of each of said heads, each of said head assemblies including a first head to read said timing track and a second head to interrogate said data carrier.

7. An optical drive according to claim 6 wherein said timing track is subdivided into frames each of which has a plurality of repetitive intermediate timing marks formed therein.

8. An optical drive according to claim 7 wherein each of said intermediate timing marks has a length measured in the direction of said track that is greater than a 50% power radius of a focused beam interrogating said timing track to recover timing data therefrom.

9. An optical drive according to claim 7 wherein each of said frames includes a pattern indicating a start of a frame.

10. An optical drive according to claim 9 wherein at least some of said frames include subcode information used to provide an address on said track.

11. An optical drive according to claim 10 wherein subcode information is recorded as data words having complementary numbers of lands and pits to maintain a self-balanced code.

12. An optical drive according to claim 9 wherein said pattern indicating a start of a frame is utilized to establish a synchronization with said clock signal.

13. An optical drive according to claim 12 wherein said intermediate clock signals are utilized to maintain synchronization with said clock signal.

14. An optical drive according to claim 6 wherein said timing track is radially offset from said data carrier.

15. An optical drive according to claim 6 wherein said timing track is spaced from said carrier along said axis.

16. An optical drive according to claim 6 wherein said timing track includes a pair of sets of timing marks, each corresponding to a respective one of a pair of timing standards.

17. An optical drive according to claim 16 wherein said sets of marks are displaced from one another along said axis and a head interrogating said timing track may be focused on one or the other of said sets of tracks.

18. An optical drive according to claim 1 wherein during recording of data on said data carrier, said head assemblies are positioned radially within a common band having a radial extent less than that of said data carrier and data is recorded as successive bands by repositioning said head assemblies.

19. An optical drive according to claim 1 wherein one of said head assemblies records data on said carrier and another of said head assemblies reads data from said carrier.

20. An optical drive according to claim 19 wherein said other head assembly reads data written by said one head to verify the data recorded.

21. An optical drive according to claim 1 wherein said clock signal is derived from the data recorded on said data carrier.

22. An optical device according to claim 21 wherein a reference clock signal is derived from the position of said head assembly relative to said data carrier and compared with the clock signal derived from said data to maintain synchronization therebetween.

23. An optical drive according to claim 22 wherein said clock signal at each location is retrieved from a look-up table and compared to that recovered from said data.

24. An optical drive according to claim 23 wherein said data includes an address which is used to access said look-up table.

25. An optical drive according to claim 18 wherein said head assemblies are positioned relative to one another by counting tracks during relative radial movement between said head assemblies.

26. An optical drive according to claim 25 wherein an address recorded by one head assembly is utilized to correlate positioning of an adjacent head.

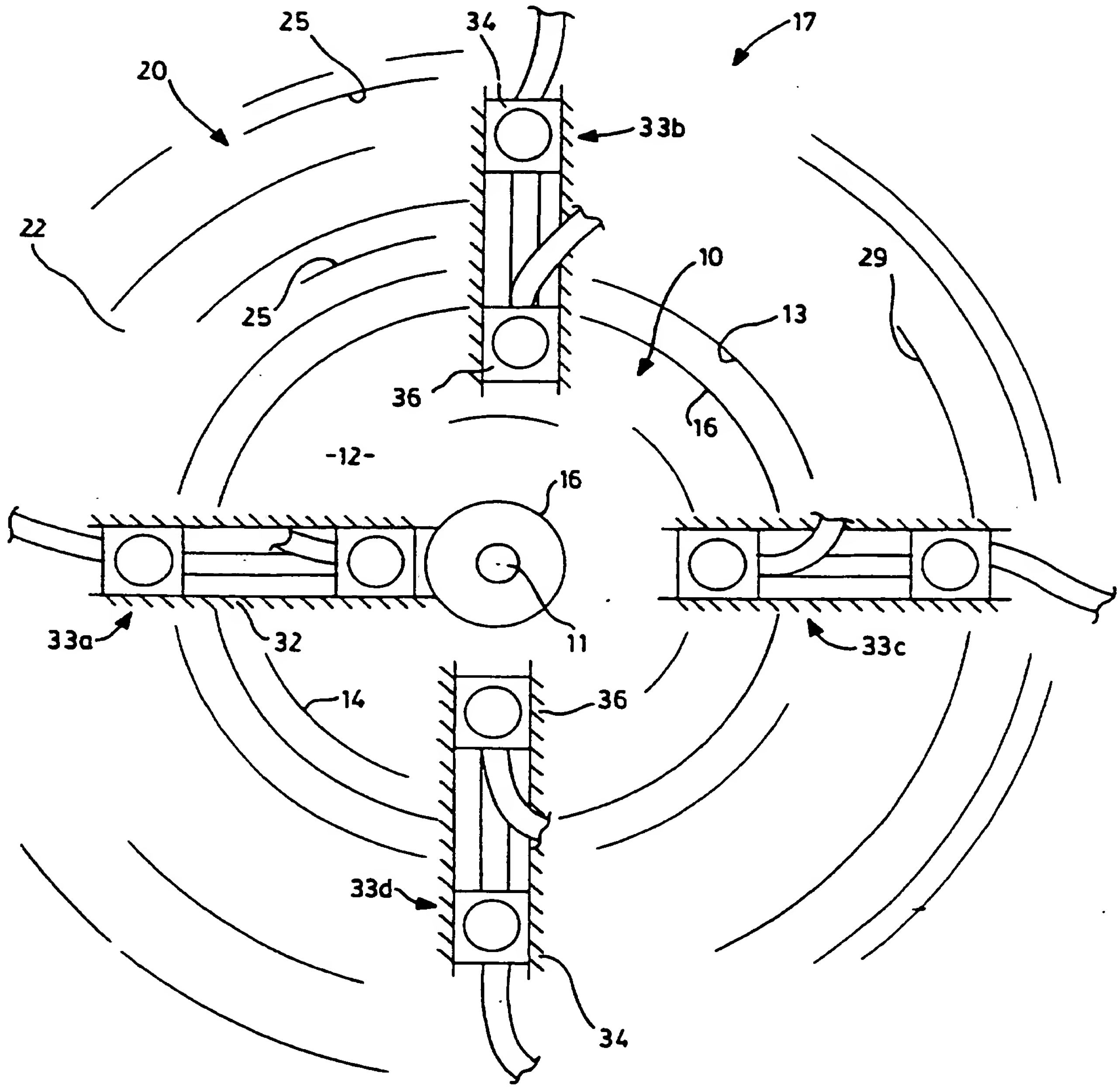


FIG. 1

SUBSTITUTE SHEET (RULE 26)

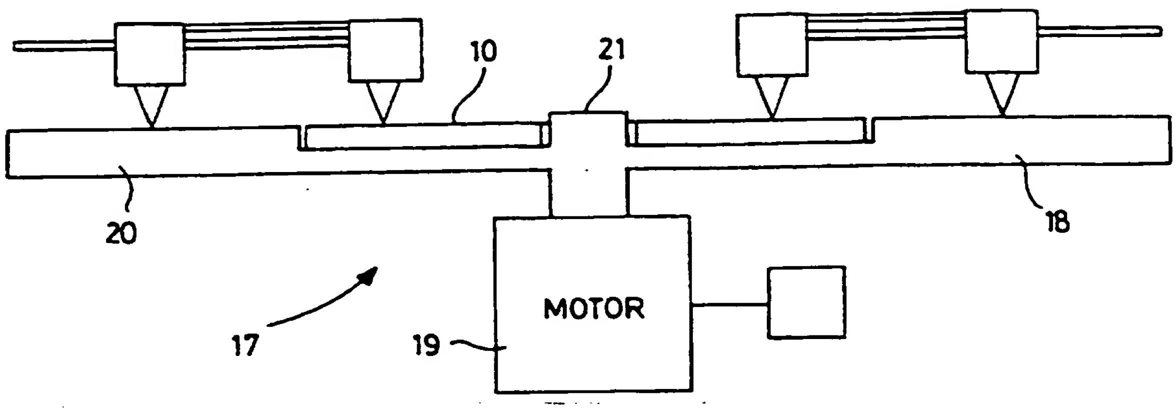


FIG. 2

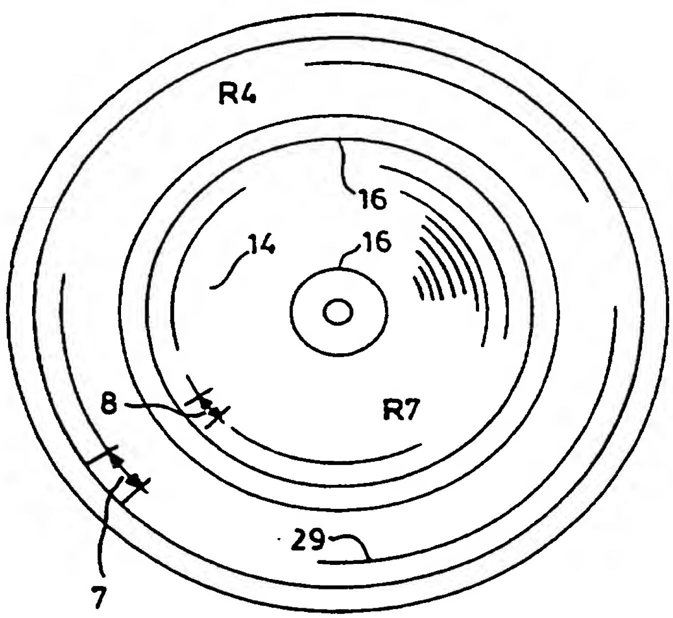


FIG. 3

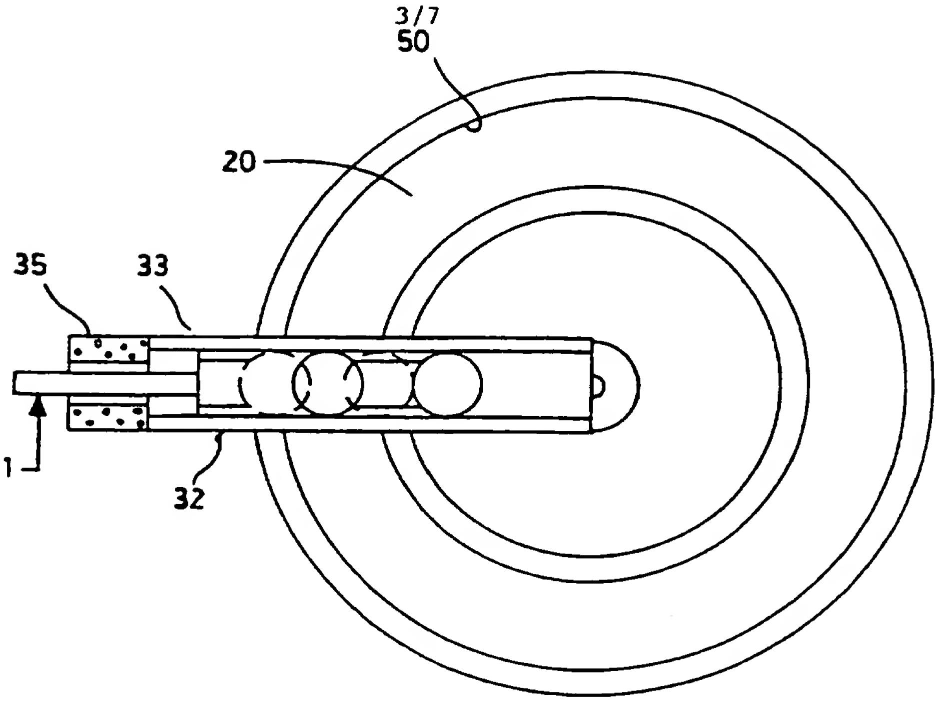


FIG. 4

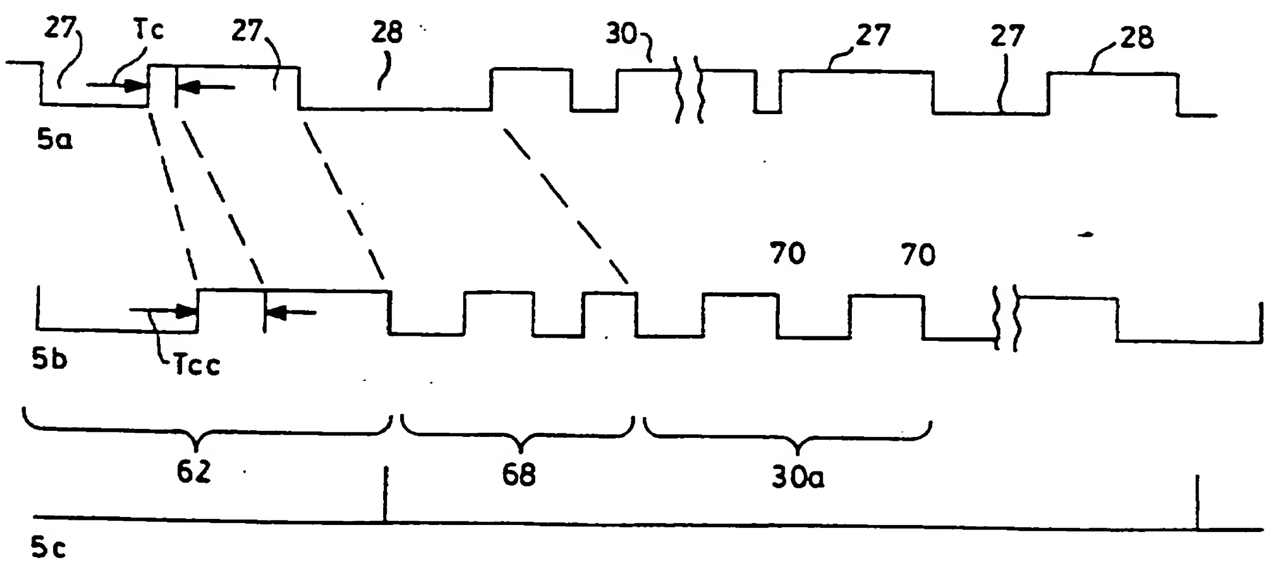
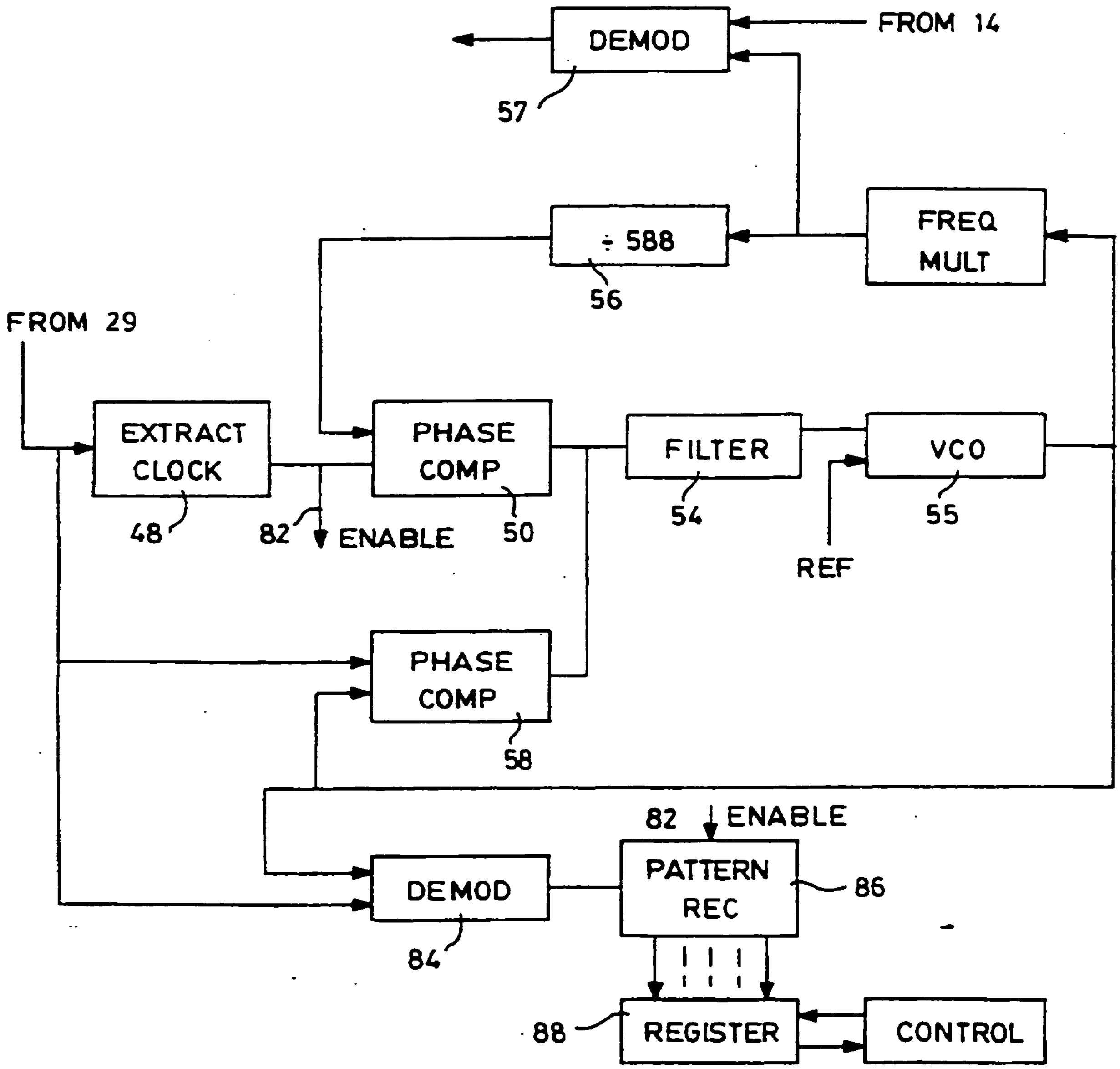


FIG. 5



DEMOD
FROM 14
57
÷ 588
FREQ MULT
56
FROM 29
EXTRACT CLOCK
PHASE COMP
FILTER
VCO
48
82
ENABLE
50
54
55
REF
PHASE COMP
58
82
ENABLE
DEMOD
PATTERN REC
86
84
88
REGISTER
CONTROL

FIG. 6

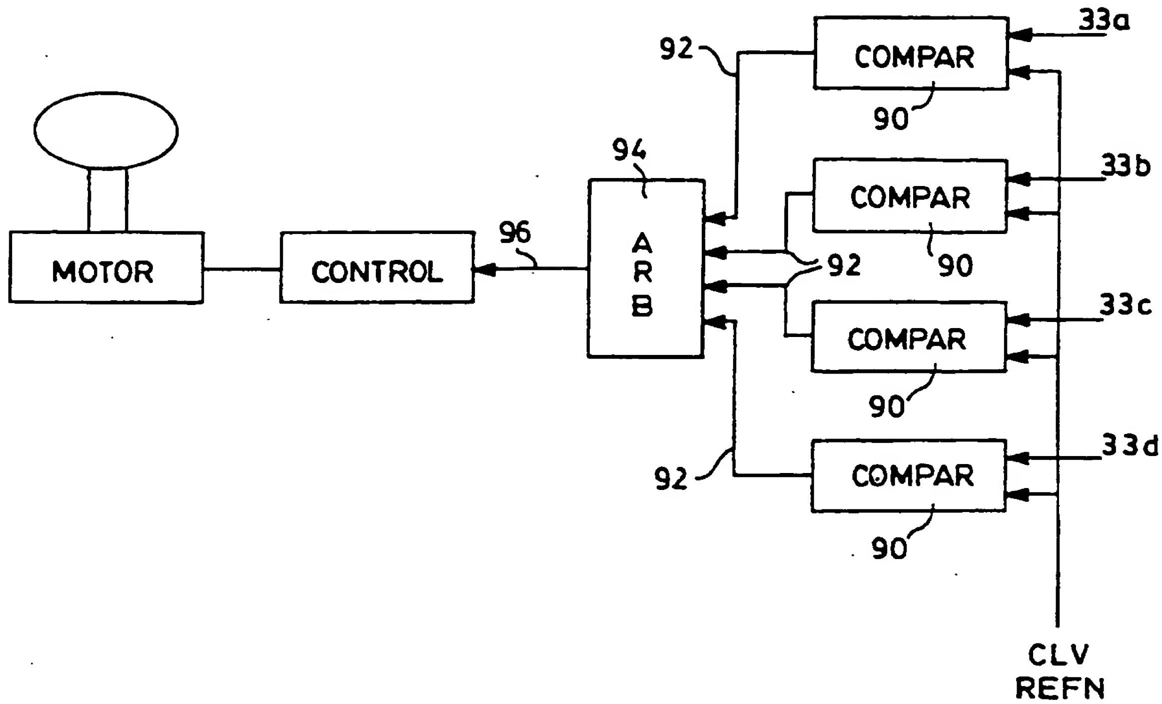


FIG. 7

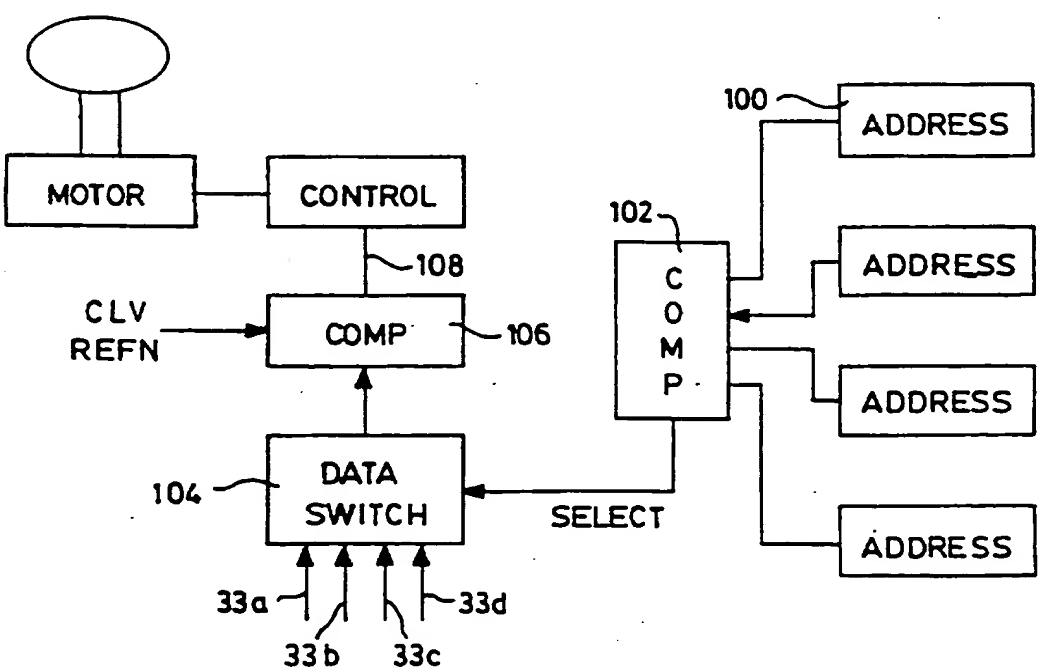


FIG. 8

SUBSTITUTE SHEET (RULE 26)

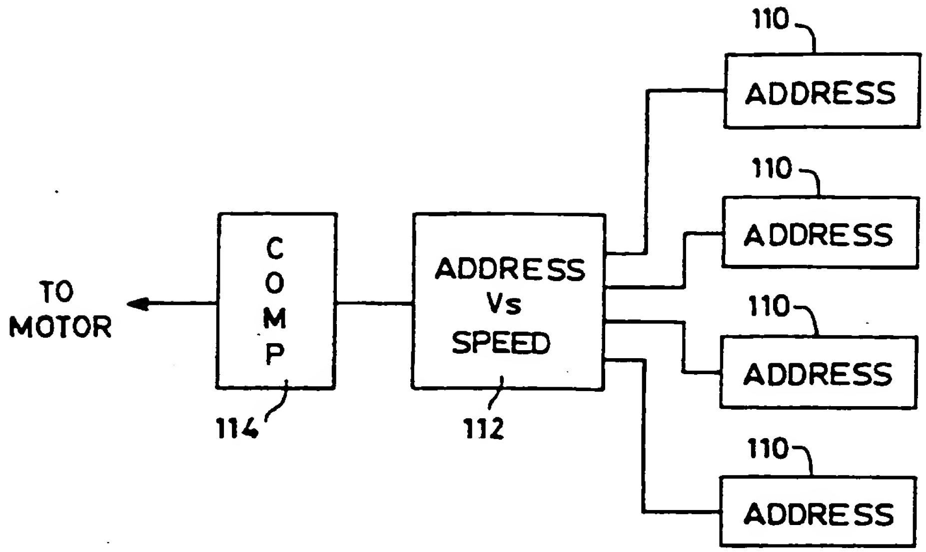


FIG. 9

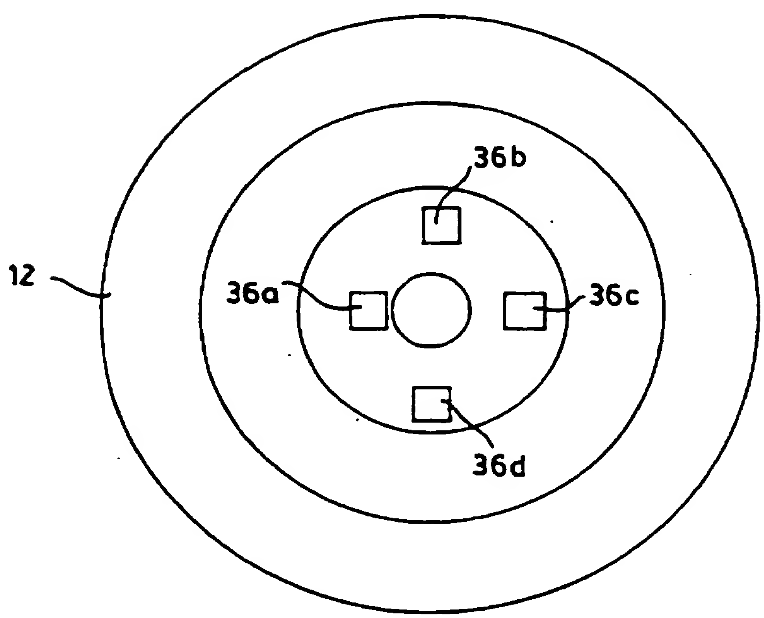


FIG. 10

SUBSTITUTE SHEET (RULE 26)

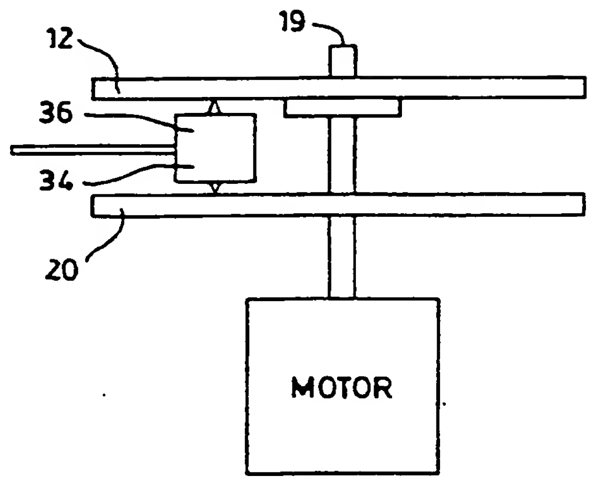


FIG. 11

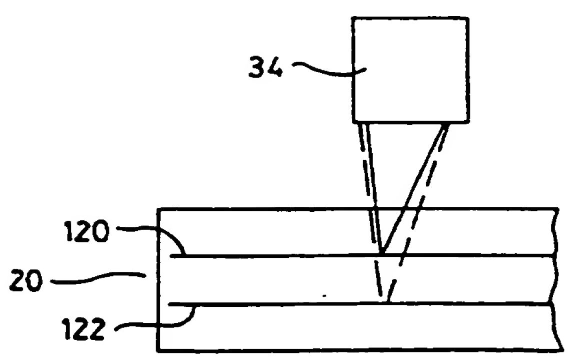


FIG. 12

INTERNATIONA[illegible] SEARCH REPORT

Intern. [illegible] ication No
PCT/CA 97/00069

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11B7/14 G11B27/11 G11B27/36

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 506 447 A (TOKYO SHIBAURA ELECTRIC CO) 30 September 1992 see page 6, line 18 - line 50; claim 6; figures 3,5	1,2,21, 22
Y		6,7,9, 10,12, 13,15,18
A		3-5

Y	EP 0 555 065 A (IBM) 11 August 1993 see abstract see page 7, line 22 - line 41 see page 11, line 10 - line 20	6,7,9, 10,12, 13,15,18

	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

1

Date of the actual completion of the international search	Date of mailing of the international search report
19 June 1997	14.07.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Annibal, P

International Application No
PCT/CA 97/00069

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 347 506 A (MATSUDO YASUNORI ET AL) 13 September 1994 see abstract; figure 1	1,2,21
A	US 5 303 215 A (DEWAR STEPHEN W ET AL) 12 April 1994 cited in the application see the whole document	6,7,9, 10,12-14
A	US 5 249 170 A (YOSHIMARU TOMOHISA ET AL) 28 September 1993 see column 4, line 56 - line 66; figure 3	6,15

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 97/00069

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0506447 A	30-09-92	JP 4301222 A US 5465244 A	23-10-92 07-11-95
EP 0555065 A	11-08-93	US 5293565 A AU 664061 B AU 3100493 A BR 9300106 A CA 2081179 A,C CN 1075230 A JP 6084287 A KR 9606847 B NZ 245391 A	08-03-94 02-11-95 05-08-93 10-08-93 05-08-93 11-08-93 25-03-94 23-05-96 21-12-95
US 5347506 A	13-09-94	JP 5128532 A	25-05-93
US 5303215 A	12-04-94	CA 1324668 A GB 2231707 A,B	23-11-93 21-11-90
US 5249170 A	28-09-93	JP 2227827 A	11-09-90